SPECIFICATION

OF

ORGANIC LIGHT EMITTING DIODES MODULE

CUSTOMER : URT-STD

Model No. : UMOH-8462N-O

Model version : 0

Document Revision : 0

CUSTOMER APPROVED SIGNATURE			

This specification need to be signed by purchaser or customer as a specification of products production and delivery from URT. Without signature of this specification , any purchase order for this model no. will be treated and considered that this specification is automatically acknowledged and accepted by purchaser or customer.

U.R.T. UNITED RADIANT TECHNOLOGY CORPORATION

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APPROVED	CHECKED	CHECKED	PREPARED	Date

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Revision record

Document Revision	Model No. Version No.	Description	Revision by
0	UMOH-8462N-O Version No. 0	3.12” PM OLED	H.F. Kuo Ken Liao 04-Oct-2010

CONTENTS:

1. BASIC SPECIFICATION

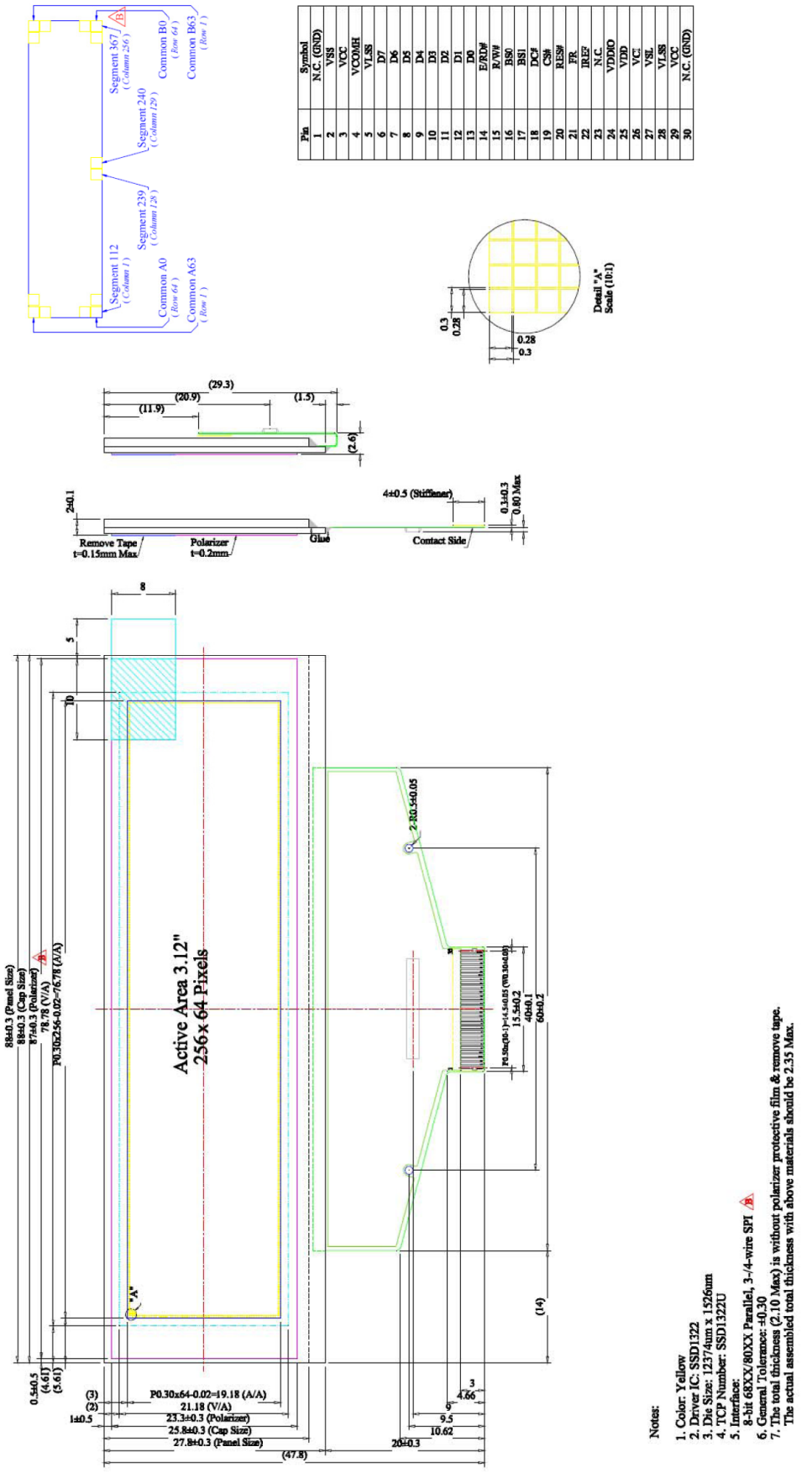
1.1 Mechanical specifications

Items	Nominal Dimension	Unit
Dot Matrix	256 x 64	Pixel
Module Size (W x H x T)	88.00 x 27.80 x 2.00	mm.
Viewing Area (W×H)	78.78 x 21.18	mm.
Active Area (W x H)	76.78 x 19.18	mm.
Dot Pitch (W×H)	0.3 x 0.3	mm.
Dot Size (W×H)	0.28 x 0.28	mm.
Driving Method	1/64	Duty
Driver IC	SSD1322	-
Interface	8-bit 68XX/80XX Parallel, 4-wire SPI, 3-wire SPI	-
Driving IC Package	TCP	-
Module Weight	9.95	g

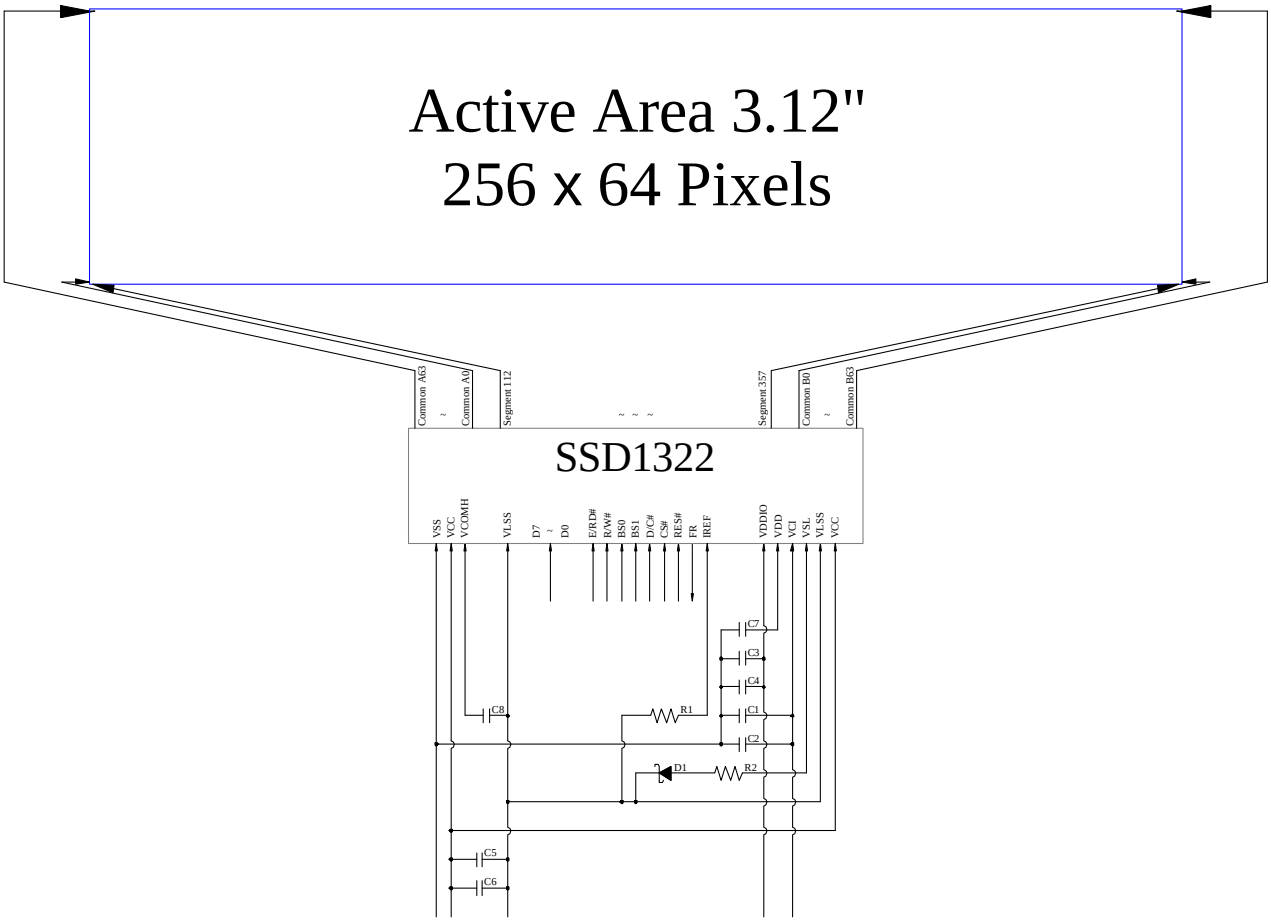
1.2 Display specification

Display	Descriptions	Note
LCD Type	3.12”OLED	-
LCD Mode	Passive Matrix Monochrome (Yellow)	-

1.3 Outline dimension



1.4 Block diagram:



MCU Interface Selection: BS0 and BS1

Pins connected to MCU interface: D7~D0, E/RD#, R/W#, D/C#, CS#, and RES#

C1, C3, C5: 0.1µF

C2, C4: 4.7µF

C6: 10µF

C7: 1µF

C8: 4.7uF / 25V Tantalum Capacitor

R1: 680kΩ, R1 = (Voltage at IREF – VSS) / IREF

R2: 50Ω, 1/4W

D1: ≈1.4V, 0.5W

1.5 Interface pin :

Pin Number	Symbol	Type	Function
1, 30	N.C. (GND)	-	**Reserved Pin (Supporting Pin)** The supporting pins can reduce the influences from stresses on the function pins. These pins must be connected to external ground.
2	VSS	P	**Ground of Logic Circuit** This is a ground pin. It also acts as a reference for the logic pins. It must be connected to external ground.
3, 29	VCC	P	**Power Supply for OEL Panel** These are the most positive voltage supply pin of the chip. They must be connected to external source.
4	VCOMH	P	**Voltage Output High Level for COM Signal** This pin is the input pin for the voltage output high level for COM signals. A tantalum capacitor should be connected between this pin and VSS.
5, 28	VLSS	P	**Ground of Analog Circuit** These are the analog ground pins. They should be connected to VSS externally.
6~13	D7~D0	I/O	**Host Data Input/Output Bus** These pins are 8-bit bi-directional data bus to be connected to the microprocessor's data bus. When serial mode is selected, D1 will be the serial data input SDIN and D0 will be the serial clock input SCLK. Unused pins must be connected to VSS except for D2 in serial mode.
14	E/RD#	I	**Read/Write Enable or Read** This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high and the CS# is pulled low. When connecting to an 80XX-microprocessor, this pin receives the Read (RD#) signal. Data read operation is initiated when this pin is pulled low and CS# is pulled low. When serial mode is selected, this pin must be connected to VSS.
15	R/W#	I	**Read/Write Select or Write** This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Pull this pin to "High" for read mode and pull it to "Low" for write mode. When 80XX interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled low and the CS# is pulled low. When serial mode is selected, this pin must be connected to VSS.

1.5 Interface Pin Connection:(continued)

<table>
<tr><th>Pin Number</th><th>Symbol</th><th>Type</th><th>Function</th></tr>
<tr><td>16
17</td><td>BS0
BS1</td><td>I</td><td>Communicating Protocol Select
These pins are MCU interface selection input. See the following table:
<table>
<tr><td></td><td>BS0</td><td>BS1</td></tr>
<tr><td>3-wire SPI</td><td>1</td><td>0</td></tr>
<tr><td>4-wire SPI</td><td>0</td><td>0</td></tr>
<tr><td>8-bit 68XX Parallel</td><td>1</td><td>1</td></tr>
<tr><td>8-bit 80XX Parallel</td><td>0</td><td>1</td></tr>
</table></td></tr>
<tr><td>18</td><td>D/C#</td><td>I</td><td>Data/Command Control
This pin is Data/Command control pin. When the pin is pulled high, the input at D7~D0 is treated as display data. When the pin is pulled low, the input at D7~D0 will be transferred to the command register. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams.</td></tr>
<tr><td>19</td><td>CS#</td><td>I</td><td>Chip Select
This pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled low.</td></tr>
<tr><td>20</td><td>RES#</td><td>I</td><td>Power Reset for Controller and Driver
This pin is reset signal input. When the pin is low, initialization of the chip is executed.</td></tr>
<tr><td>21</td><td>FR</td><td>O</td><td>Frame Frequency Triggering Signal
This pin will send out a signal that could be used to identify the driver status. Nothing should be connected to this pin. It should be left open individually.</td></tr>
<tr><td>22</td><td>IREF</td><td>I</td><td>Current Reference for Brightness Adjustment
This pin is segment current reference pin. A resistor should be connected between this pin and VSS. Set the current lower than 10uA.</td></tr>
<tr><td>23</td><td>N.C.</td><td>-</td><td>Reserved Pin
The N.C. pin between function pins are reserved for compatible and flexible design.</td></tr>
<tr><td>24</td><td>VDDIO</td><td>P</td><td>Power Supply for I/O Pin
This pin is a power supply pin of I/O buffer. It should be connected to VCI or external source. All I/O signal should have VIH reference to VDDIO. When I/O signal pins (BS0~BS1, D0~D7, control signals…) pull high, they should be connected to VDDIO.</td></tr>
<tr><td>25</td><td>VDD</td><td>P</td><td>Power Supply for Core Logic Circuit
This is a voltage supply pin. It can be supplied externally (within the range of 2.4~2.6V) or regulated internally from VCI. A capacitor should be connected between this pin & VSS under all circumstances.</td></tr>
</table>

1.5 Interface Pin Connection:(continued)

Pin Number	Symbol	I/O	Function
26	VCI	P	**Power Supply for Operation** This is a voltage supply pin. It must be connected to external source & always be equal to or higher than VDD & VDDIO.
27	VSL	P	**Voltage Output Low Level for SEG Signal** This is segment voltage reference pin. When external VSL is not used, this pin should be left open. When external VSL is used, this pin should connect with resistor and diode to ground.

2. ELECTRICAL CHARACTERISTICS

2.1 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage for Operation	V_{CI}	-0.3	4	V	1, 2
Supply Voltage for Logic	V_{DD}	-0.5	2.75	V	1, 2
Supply Voltage for I/O Pins	V_{DDIO}	-0.5	V_{CI}	V	1, 2
Supply Voltage for Display	V_{CC}	-0.5	16	V	1, 2
Operating Current for V_{CC}	I_{CC}	-	60	mA	1, 2
Operating Temperature	T_{OP}	-40	85	°C	3
Storage Temperature	T_{STG}	-40	90	°C	3
Life Time (80 cd/m^2)		40,000	-	hour	4

Note 1: All the above voltages are on the basis of "VSS = 0V".

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 3. "Optics & Electrical Characteristics". If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

Note 3: The defined temperature ranges do not include the polarizer. The maximum withstood temperature of the polarizer should be 80°C.

Note 4: V_{CC} = 12V, T_a = 25°C, 50% Checkerboard.
Software configuration follows Section 4.4 Initialization.
End of lifetime is specified as 50% of initial brightness reached. The average operating lifetime at room temperature is estimated by the accelerated operation at high temperature conditions.

2.2 DC Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage for Operation	V_{CI}		2.4	2.8	3.5	V
Supply Voltage for Logic	V_{DD}		2.4	2.5	2.6	V
Supply Voltage for I/O Pins	V_{DDIO}		1.65	1.8	V_{CI}	V
Supply Voltage for Display	V_{CC}	Note 5	11.5	12	12.5	V
High Level Input	V_{IH}		$0.8\times V_{DDIO}$	-	V_{DDIO}	V
Low Level Input	V_{IL}		0	-	$0.2\times V_{DDIO}$	V
High Level Output	V_{OH}	I_{out} = 100μA, 3.3MHz	$0.9\times V_{DDIO}$	-	V_{DDIO}	V
Low Level Output	V_{OL}	I_{out} = 100μA, 3.3MHz	0	-	$0.1\times V_{DDIO}$	V
Operating Current for V_{CI}	I_{CI}		-	180	300	μA
Operating Current for V_{CC}	I_{CC}	Note 6	-	28.1	35.1	mA
		Note 7	-	47.7	59.7	mA
Sleep Mode Current for V_{CI}	$I_{CI, SLEEP}$		-	20	100	μA
Sleep Mode Current for V_{CC}	$I_{CC, SLEEP}$		-	2	10	μA

Note 5: Brightness (L_{br}) and Supply Voltage for Display (V_{CC}) are subject to the change of the panel characteristics and the customer's request.

Note 6: V_{CI} = 2.8V, V_{CC} = 12V, 50% Display Area Turn on.

Note 7: V_{CI} = 2.8V, V_{CC} = 12V, 100% Display Area Turn on.

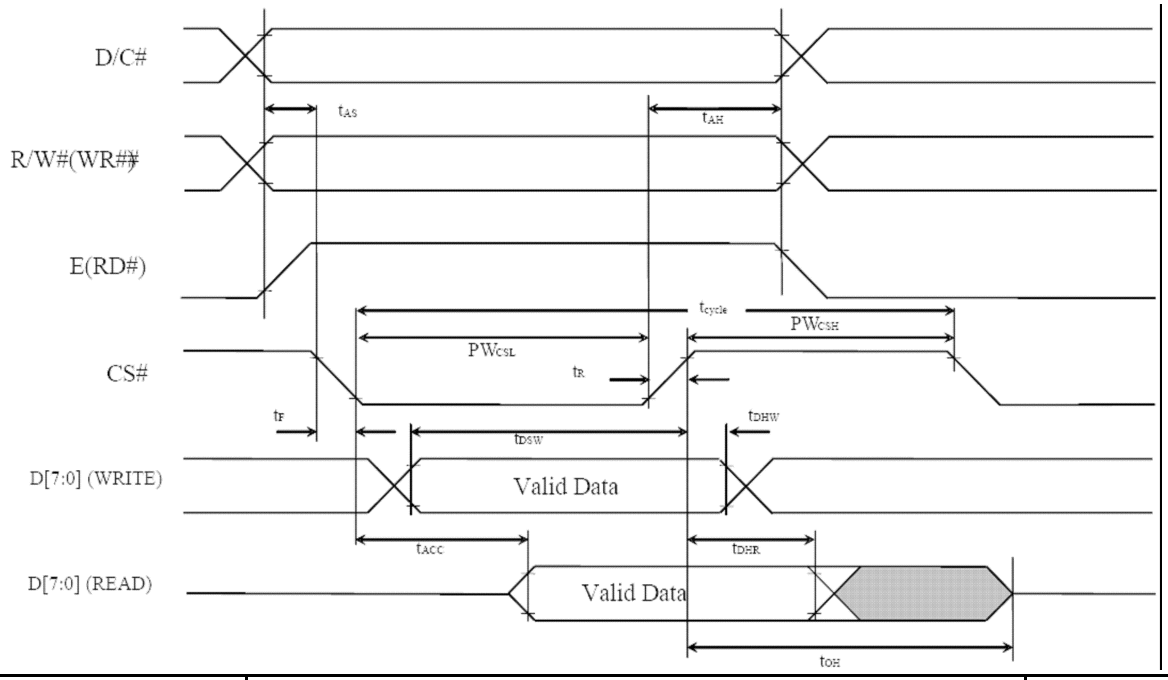
* Software configuration follows Section 4.4 Initialization.

2.3 AC Characteristics

2.3.1 68XX-Series MPU Parallel Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	ns
t_{AS}	Address Setup Time	10	-	ns
t_{AH}	Address Hold Time	0	-	ns
t_{DSW}	Write Data Setup Time	40	-	ns
t_{DHW}	Write Data Hold Time	7	-	ns
t_{DHR}	Read Data Hold Time	20	-	ns
t_{OH}	Output Disable Time	-	70	ns
t_{ACC}	Access Time	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (Read)	120	-	ns
	Chip Select Low Pulse Width (Write)	60		
PW_{CSH}	Chip Select High Pulse Width (Read)	60	-	ns
	Chip Select High Pulse Width (Write)	60		
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

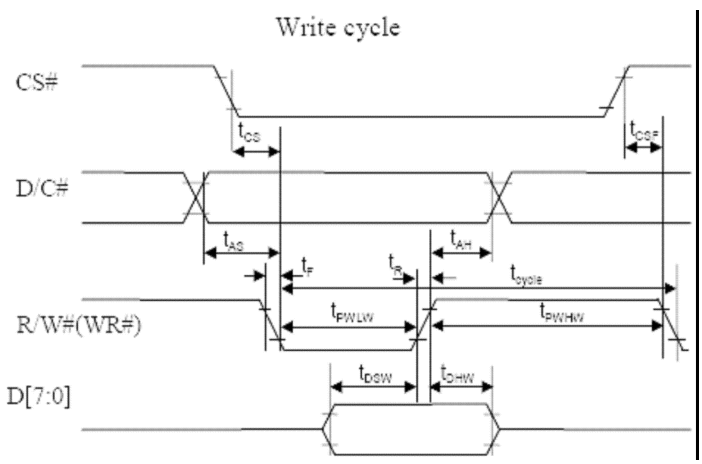
* (V_{DD} - V_{SS} = 2.4V to 2.6V, V_{DDIO} = 1.6V, V_{CI} = 2.8V, T_a = 25°C)

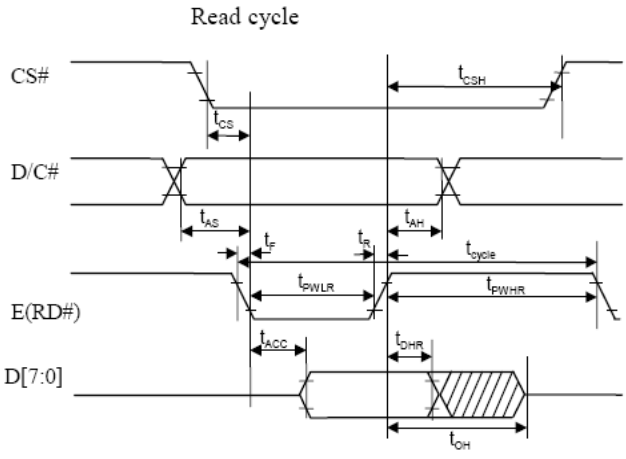


2.3.2 80XX-Series MPU Parallel Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	ns
t_{AS}	Address Setup Time	10	-	ns
t_{AH}	Address Hold Time	0	-	ns
t_{DSW}	Write Data Setup Time	40	-	ns
t_{DHW}	Write Data Hold Time	7	-	ns
t_{DHR}	Read Data Hold Time	20	-	ns
t_{OH}	Output Disable Time	-	70	ns
t_{ACC}	Access Time	-	140	ns
t_{PWLR}	Read Low Time	150	-	ns
t_{PWLW}	Write Low Time	60	-	ns
t_{PWHR}	Read High Time	60	-	ns
t_{PWHW}	Write High Time	60	-	ns
t_{CS}	Chip Select Setup Time	0	-	ns
t_{CSH}	Chip Select Hold Time to Read Signal	0	-	ns
t_{CSF}	Chip Select Hold Time	20	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

* (V_{DD} - V_{SS} = 2.4V to 2.6V, V_{DDIO} = 1.6V, V_{CI} = 2.8V, T_a = 25°C)

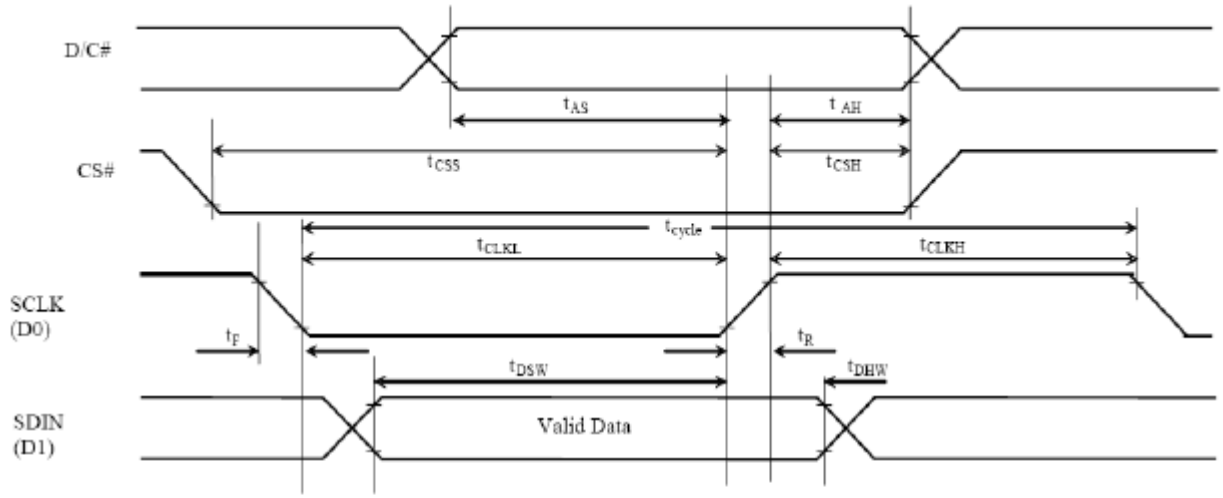


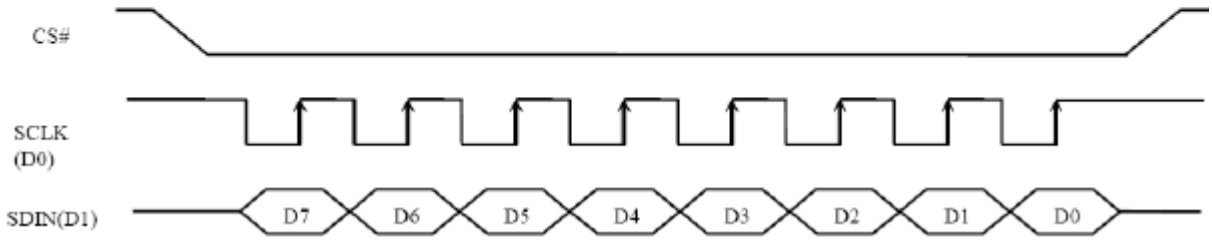


2.3.3 Serial Interface Timing Characteristics(4wire SPI):

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	ns
t_{AS}	Address Setup Time	15	-	ns
t_{AH}	Address Hold Time	15	-	ns
t_{CSS}	Chip Select Setup Time	20	-	ns
t_{CSH}	Chip Select Hold Time	10	-	ns
t_{DSW}	Write Data Setup Time	15	-	ns
t_{DHW}	Write Data Hold Time	15	-	ns
t_{CLKL}	Clock Low Time	20	-	ns
t_{CLKH}	Clock High Time	20	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

* (V_{DD} - V_{SS} = 2.4V to 2.6V, V_{DDIO} = 1.6V, V_{CI} = 2.8V, T_a = 25°C)

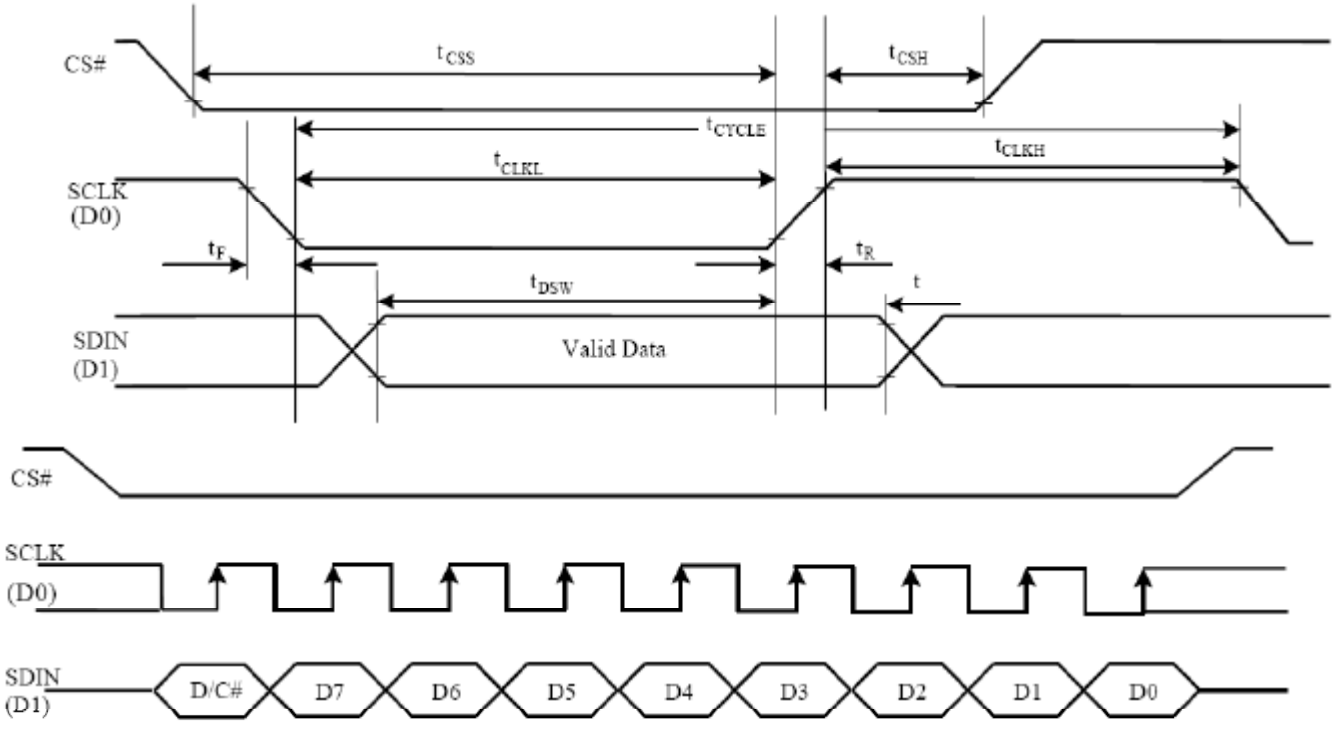




2.3.4 Serial Interface Timing Characteristics: (3-wire SPI):

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	ns
t_{AS}	Address Setup Time	15	-	ns
t_{AH}	Address Hold Time	15	-	ns
t_{CSS}	Chip Select Setup Time	20	-	ns
t_{CSH}	Chip Select Hold Time	10	-	ns
t_{DSW}	Write Data Setup Time	15	-	ns
t_{DHW}	Write Data Hold Time	15	-	ns
t_{CLKL}	Clock Low Time	20	-	ns
t_{CLKH}	Clock High Time	20	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

* (V_{DD} - V_{SS} = 2.4V to 2.6V, V_{DDIO} = 1.6V, V_{CI} = 2.8V, T_a = 25°C)



2.4 Functional Specification

2.4.1. Commands

Refer to the Technical Manual for the SSD1322

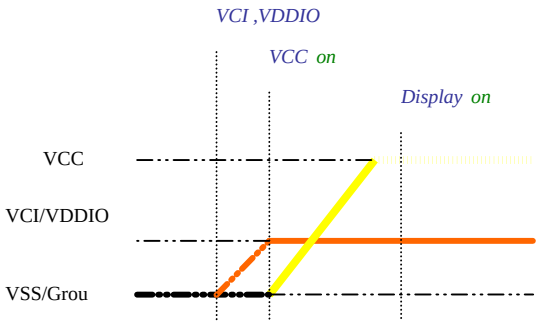
2.4.2 Power down and Power up Sequence

To protect OEL panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off.

It gives the OEL panel enough time to complete the action of charge and discharge before/after the operation.

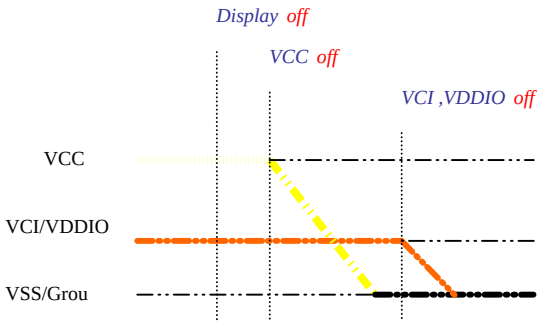
2.4.2.1 Power up Sequence:

1. Power up V_{CI} & V_{DDIO}
2. Send Display off command
3. Initialization
4. Clear Screen
5. Power up V_{CC}
6. Delay 100ms
   (When V_{CC} is stable)
7. Send Display on command



2.4.2.2 Power down Sequence:

1. Send Display off command
2. Power down V_{CC}
3. Delay 100ms
   (When V_{CC} is reach 0 and panel is completely discharges)
4. Power down V_{CI} & V_{DDIO}



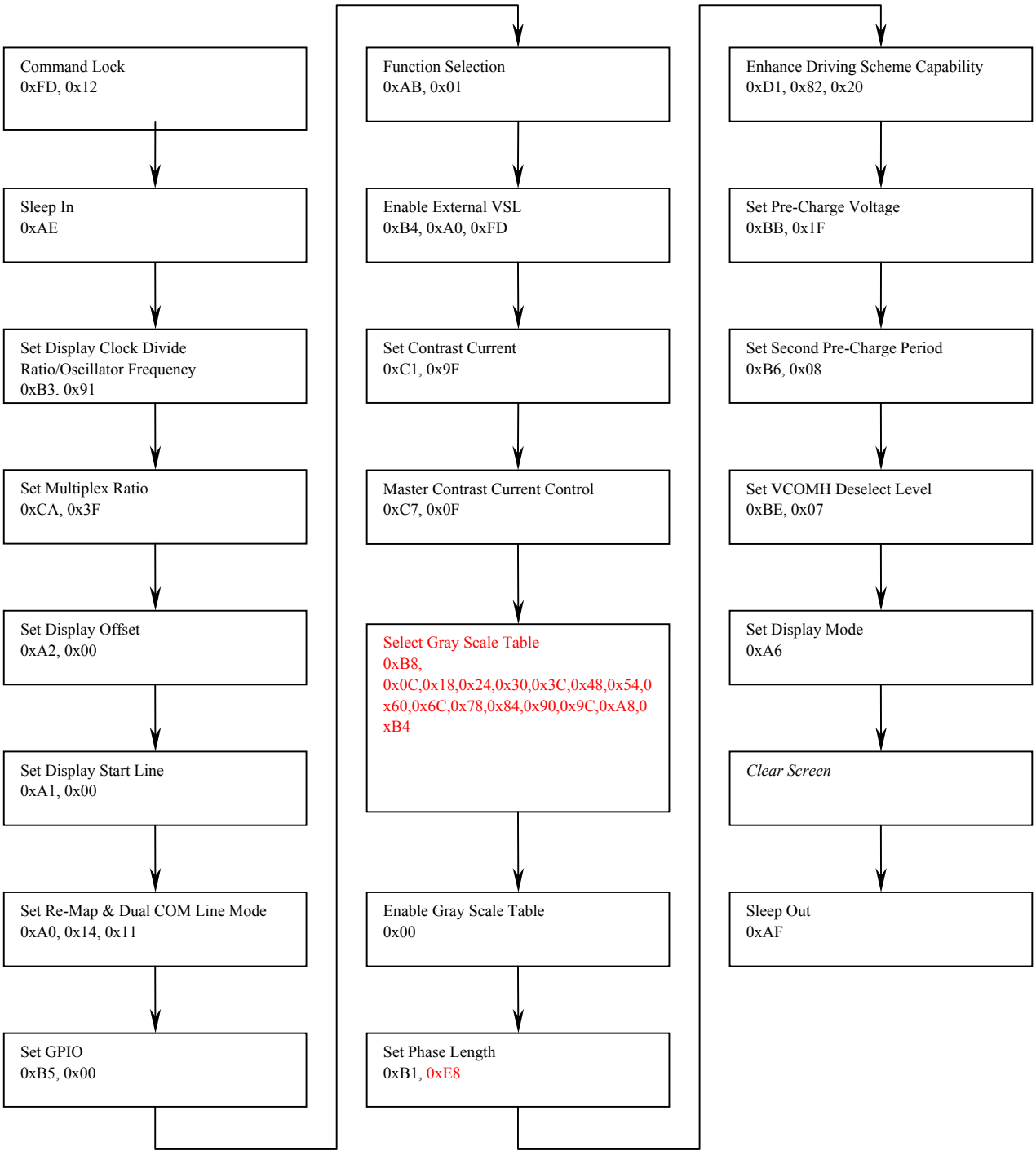
2.4.3 Reset Circuit

When RES# input is low, the chip is initialized with the following status:

1. Display is OFF
2. 480×128 Display Mode
3. Normal segment and display data column and row address mapping (SEG0 mapped to column address 00h and COM0 mapped to row address 00h)
4. Display start line is set at display RAM address 0
5. Column address counter is set at 0
6. Normal scan direction of the COM outputs
7. Contrast control registers is set at 7Fh

2.4.4 Actual Application Example

Command usage and explanation of an actual example
<Initialization>



If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

3. OPTICAL CHARACTERISTICS

3.1 Characteristics

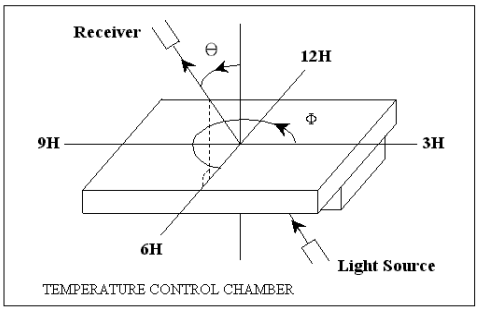
Electrical and Optical Characteristics

No.	Item	symbol / temp.		Min.	Typ.	Max.	Unit	Note
1	View Angle			>160	-	-	degree	3
2	Dark Room Contrast	Cr	25 ℃	-	>2000:1	-	-	4
3	Yellow x-code	Yx		0.47	0.50	0.53		5
	Yellow y-code	Yy		0.46	0.49	0.52		
	Brightness	Y		60	80	-	cd/m^2	

3.2 Definition of optical characteristics

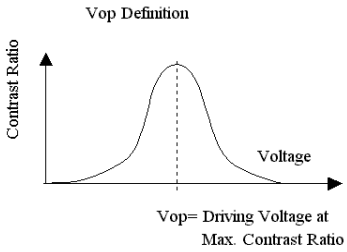
Measurement condition :

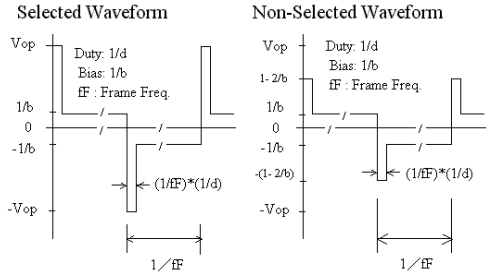
Transmissive and Transflective type



PHOTAL LCD-5000

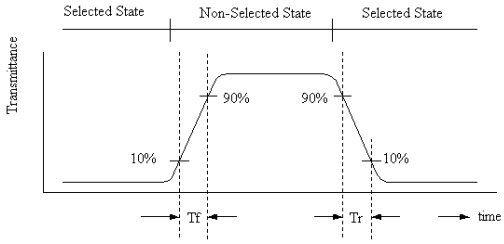
[Note 1] Definition of LCD Driving Vop and Waveform :



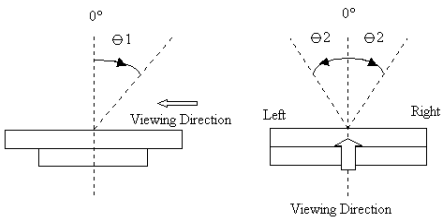


[Note 2] Definition of Response Time

for Positive type :

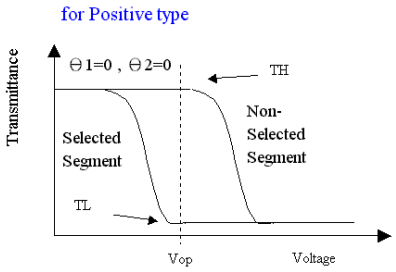


[Note 3] Definition of Viewing Angle :



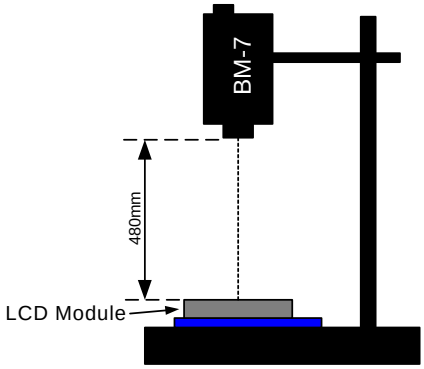
[Note 4] Definition of Contrast Ratio :

for Positive type

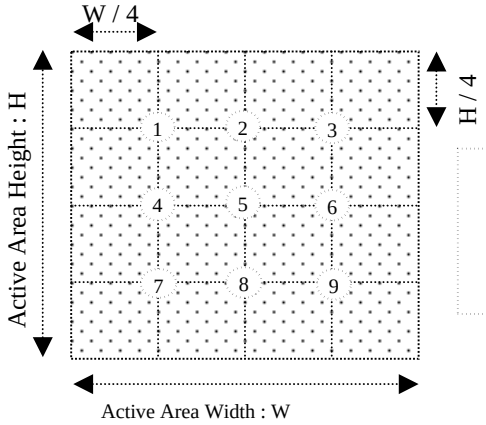


$$\text{Contrast Ratio} = \frac{TH}{TL}$$

[Note 5] Definition of measurement of Color Chromaticity and Brightness

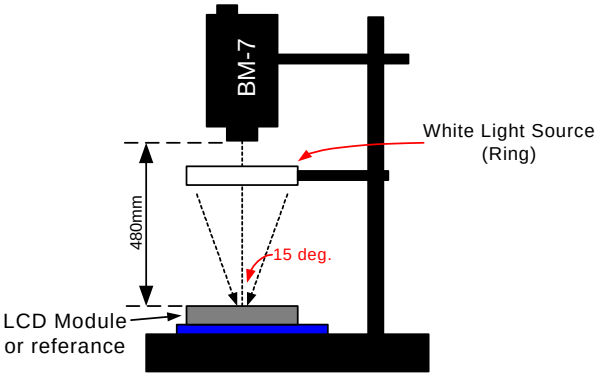


[Note 6] Definition of Brightness Uniformity



$$\text{Brightness Uniformity} = \frac{\text{Minimum Brightness of Point 1~9}}{\text{Maximum Brightness of Point 1~9}}$$

[Note 7] Definition of Measurement of Reflectance



4. RELIABILITY :

Item No	Items	Condition
1	High temperature operating	85 ℃ , 200 hours
2	Low temperature operating	-40 ℃ , 200 hours
3	High temperature storage	90 ℃ , 200 hours
4	Low temperature storage	-40 ℃ , 200 hours
5	High temperature & humidity storage	60℃, 90%RH, 100 hours
6	Thermal Shock storage	-40℃, 30min.<=> 90℃, 30min. 10 Cycles
7	Vibration test	10 => 55 =>10 => 55 => 10 Hz , within 1 minute Amplitude : 1.5mm. 15 minutes for each Direction (X,Y,Z)
8	Drop test	Packed, 100CM free fall, 6 sides, 1 corner, 3edges
9	Life time	50,000 hours 25℃ , 60%RH , specification condition driving

* One single product test for only one item.

* Judgment after test : keep in room temperature for more than 2 hours.

- Current consumption < 2 times of initial value
- Contrast > 1/2 initial value
- Function : work normally

5. PRODUCT HANDLING AND APPLICATION

☐ PRECAUTION FOR HANDLING OLED MODULE

- The LCD module contains a C-MOS LSI. People who operate the OLED module should wear ESD protection eguipement to prevent ESD hurt on products.
- Do not input any signal before power is turned on.
- Do not take OLED module from its packaging bag until it is assembled.
- Peel off the OLED module protective film slowly since static electricity may be generated.
- Pay attention to the humidity of the work shop, 50~60%RH is satisfactory.
- Use a non-leak iron for soldering OLED module.
- Do not touch the display surface or connection terminals area with bare hands.Smudges on the display surface reduce the insulation between terminals.
- Cautions for soldering to OLED module:

  Condition for soldering I/O terminals:
  Temperature at iron tip :350℃±15℃.
  Soldering time : 3~4sec./ terminals.
  Type of solder : Eutectic solder(rosin flux filled).

☐ PRECAUTION FOR STORING OLED MODULE

- To avoid degradation of the device , do not store the module under the conditions of direct sunlight , high temperature or high humidity . Keep the module in bags designed to prevent static electricity charging under low temperature / normal humidity conditions(avoid high temperature / high humidity and low temperature below 0℃)
- Never use the LCD , LCM under 45 Hz , the liquid crystal will decomposition and cause permently damage on display !!

☐ USING ON MEDICAL CARE , SAFETY OR HAZARDOUS APPLICATION OR SYSTEM

- For the application in medical care, safety and hazardous prodcuts or systems, an authorization from URT is required. URT will not responsible for any damage or loss which caused by the products without any authorization given by URT.
- This product is not allowed to be designed and used for military application and/or purpose.
- The delivery of this product to the countries and/or regions where the embargoes are imposed by U.N. is prohibited.
- The application and delivery of this product must comply with Startegic High-Tech Commodities (SHTC) export control and the sales to the embargoed and/or sanctioned countries or regions are strictly prohibited.

6. DATE CODE OF PRODUCTS

- Date code will be shown on each product :

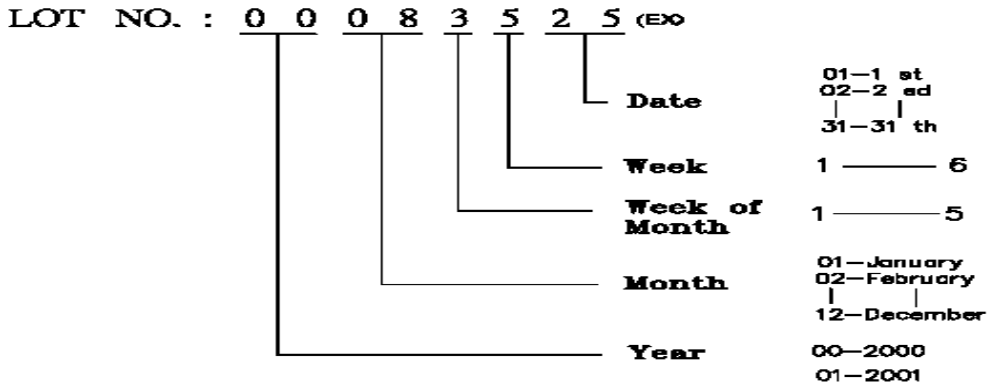
- **YY MM DD - XXXX**

  Year Month Day - Production lots

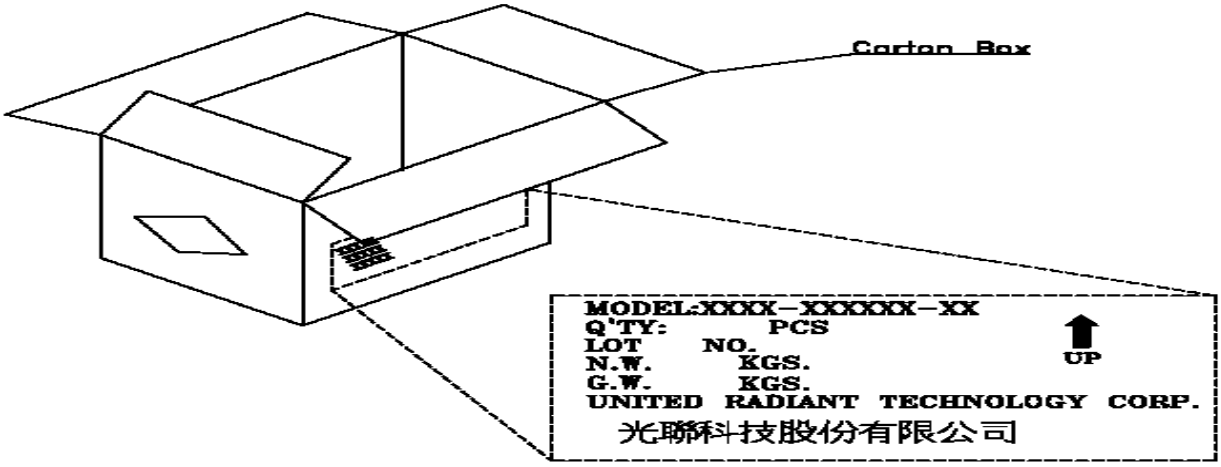
- Example: 090508 - 0 0 0 3 ==>Year 2009, May.,08rd , Batch no.03

7. PACKING

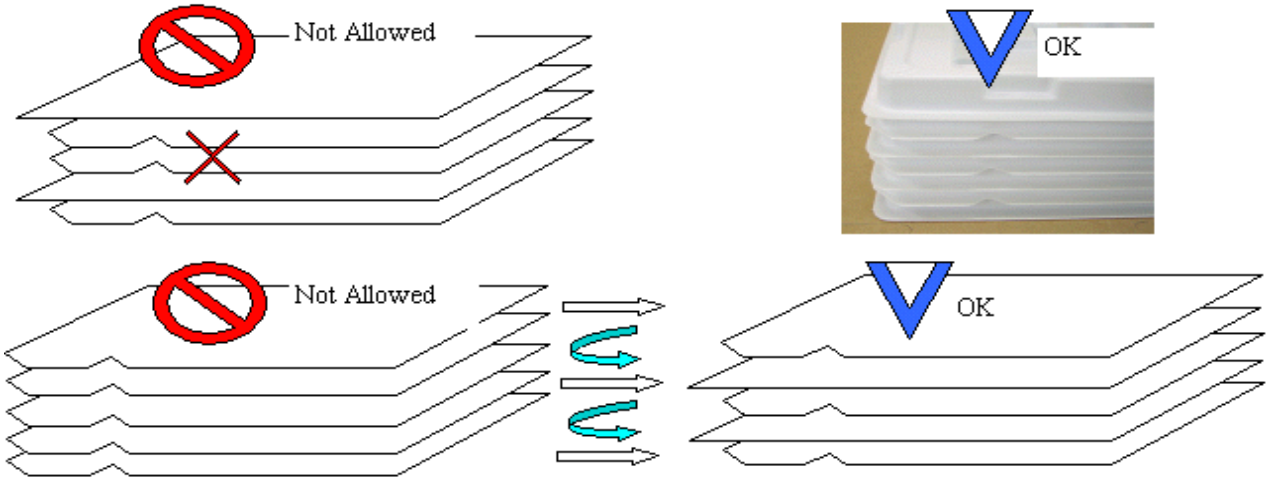
Instruction of lot number:



Lable of carton:



Packing tray must be stacked with alternated direction to each others.
To tacks packing trays in same direction will cause product damaged.



MODEL NO: UM*

T.B.D pcs / Tray

T.B.D Tray / Box

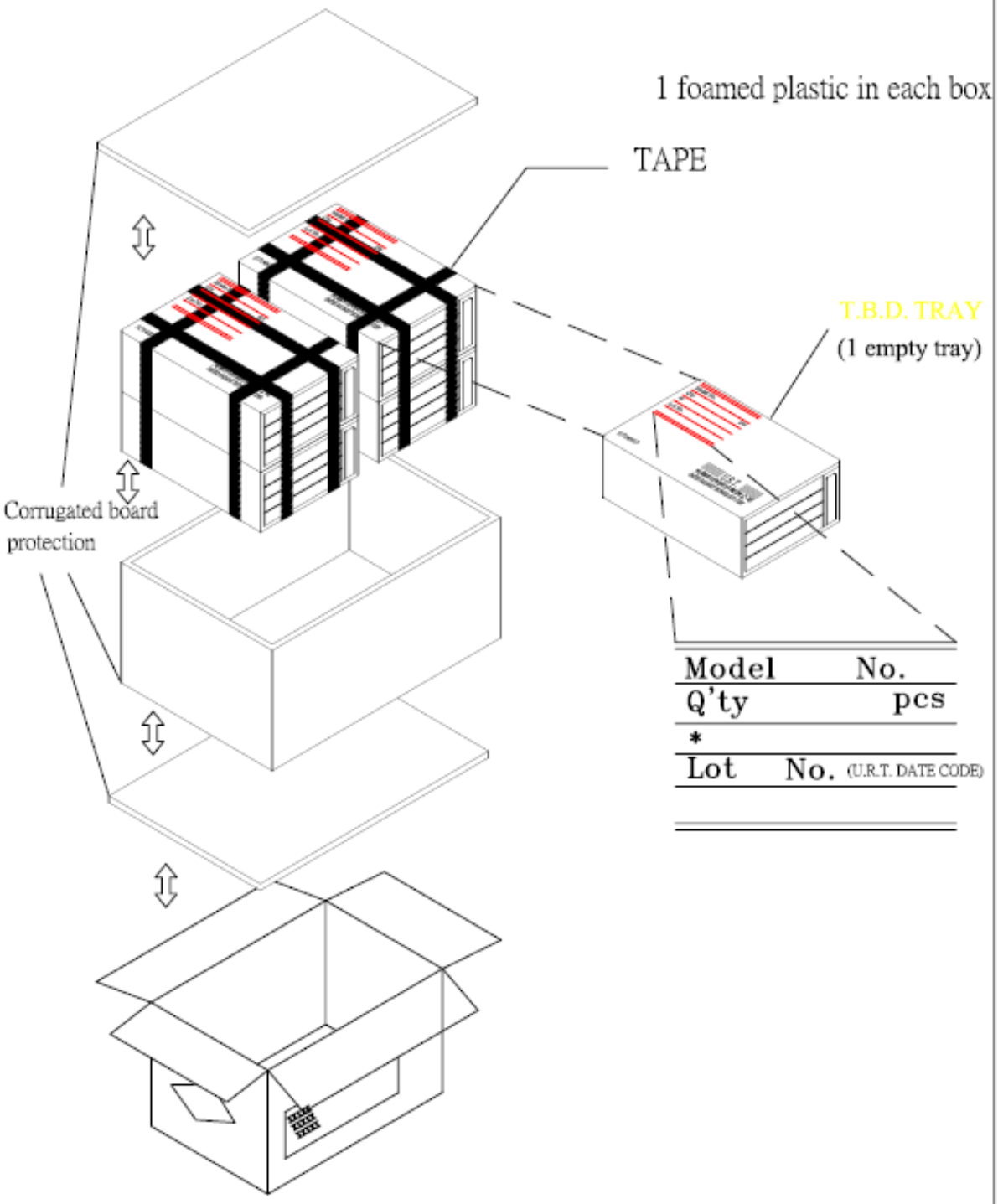
T.B.D Box / Carton

T.B.D pcs / Carton

NOTE:

(1)Be warned ,the direction of the tray has to turn it by 180 degree before stack it up.Otherwise, it will be packager's responsibility!!

(2)Safe Stack : 5 cartons only



8. INSPECTION STANDARD

8.1. QUALITY :

THE QUALITY OF GOODS SUPPLIED TO PURCHASER SHALL COME UP TO THE FOLLOWING STANDARD.

8.1.1. THE METHOD OF PRESERVING GOODS

AFTER DELIVERY OF GOODS FROM U.R.T. TO PURCHASER. PURCHASER SHALL CONTROL THE LCM AT -10 ℃ 40 ℃ ,AND IT MIGHT BE DESIRABLE TO KEEP AT THE NORMAL ROOM TEMPERATURE AND HUMIDITY UNTIL INCOMING INSPECTION OR THROWING INTO PROCESS LINE.

8.1.2. INCOMING INSPECTION

(A) THE METHOD OF INSPECTION

IF PURCHASER MAKE AN INCOMING INSPECTION , A SAMPLING PLAN SHALL BE APPLIED ON THE CONDITION THAT QUALITY OF ONE DELIVERY SHALL BE REGARDED AS ONE LOT.

(B) THE STANDARD OF QUALITY

ISO-2859-1 (or MIL-STD-105E) , LEVEL Ⅱ SINGLE PLAN.

CLASS	AQL(%)
CRITICAL	0.4 %
MAJOR	0.65 %
MINOR	1.5 %
TOTAL	1.5 %

EVERY ITEM SHALL BE INSPECTED ACCORDING TO THE CLASS.

(C) MEASURE

IF AS THE RESULT OF ABOVE RECEIVING INSPECTION , A LOT OUT IS DISCOVERED. PURCHASER SHALL BE INFORM SELLER OF IT WITHIN SEVEN DAYS. BUT FIRST SHIPMENT WITHIN FOURTEEN DAYS.

8.1.3. WARRANTY POLICY

U.R.T. WILL PROVIDE ONE-YEAR WARRANTY FOR THE PRODUCTS ONLY IF UNDER SPECIFICATION OPERATING CONDITIONS. U.R.T. WILL REPLACE NEW PRODUCTS FOR THESE DEFECT PRODUCTS WHICH UNDER WARRANTY PERIOD AND BELONG TO THE RESPONSIBILITY OF U.R.T.

8.2. CHECKING CONDITION

8.2.1. CHECKING DIRECTION SHALL BE IN THE 45 DEGREE AREA TO FACE THE SAMPLE.

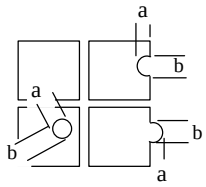
8.2.2. CHECKER SHALL SEE OVER 30 cm. WITH BARE EYES FAR FROM SAMPLE AND USING 2 PCS. OF 20W FLUORESCENT LAMP.

8.3. INSPECTION PLAN :

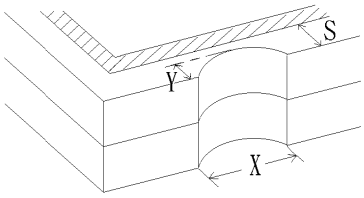
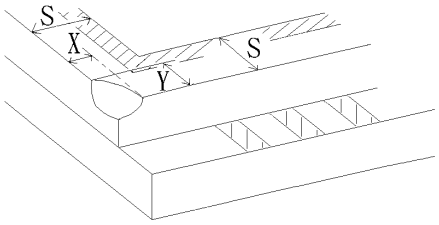
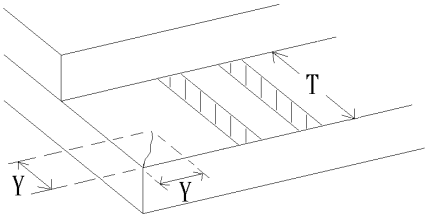
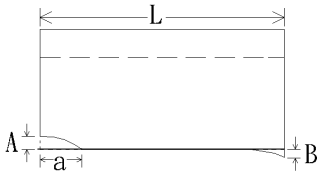
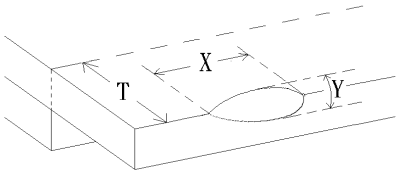
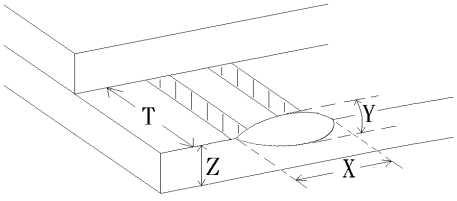
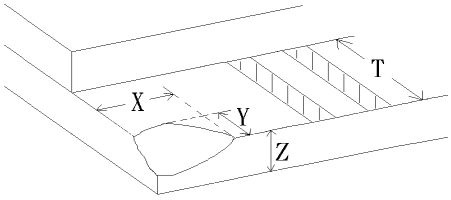
CLASS	ITEM	JUDGEMENT	CLASS
PACKING & INDICATE	1. OUTSIDE AND INSIDE PACKAGE	"MODEL NO." , "LOT NO." AND "QUANTITY" SHOULD INDICATE ON THE PACKAGE.	Minor
	2. MODEL MIXED AND QUANTITY	OTHER MODEL MIXED.....REJECTED QUANTITY SHORT OR OVER.....REJECTED	Critical
	3. PRODUCT INDICATION	"MODEL NO." SHOULD INDICATE ON THE PRODUCT	Major
ASSEMBLY	4. DIMENSION, LCD GLASS SCRATCH AND SCRIBE DEFECT.	ACCORDING TO SPECIFICATION OR DRAWING.	Major
APPEARANCE	5. VIEWING AREA	POLARIZER EDGE OR LCD'S SEALING LINE IS VISABLE IN THE VIEWING AREA ……..REJECTED	Minor
	6. BLEMISH、BLACK SPOT、 WHITE SPOT IN THE LCD AND LCD GLASS CRACKS	ACCORDING TO STANDARD OF VISUAL INSPECTION (INSIDE VIEWING AREA)	Minor
	7. BLEMISH、BLACK SPOT WHITE SPOT AND SCRATCH ON THE POLARIZER	ACCORDING TO STANDARD OF VISUAL INSPECTION (INSIDE VIEWING AREA)	Minor
	8. BUBBLE IN POLARIZER	ACCORDING TO STANDARD OF VISUAL INSPECTION (INSIDE VIEWING AREA)	Minor
	9. LCD'S RAINBOW COLOR	STRONG DEVIATION COLOR (OR NEWTON RING) OF LCD.....REJECTED. OR ACCORDING TO LIMITED SAMPLE (IF NEEDED, AND INSIDE VIEWING AREA)	Minor
ELECTRICAL	10. ELECTRICAL AND OPTICAL CHARACTERISTICS (CONTRAST、VOP、 CHROMATICITY … ETC)	ACCORDING TO SPECIFICATION OR DRAWING . (INSIDE VIEWING AREA)	Critical
	11.MISSING LINE	MISSING DOT、LINE、CHARACTER ....REJECTED	Critical
	12.SHORT CIRCUIT、 WRONG PATTERN DISPLAY	NON DISPLAY、WRONG PATTERN DISPLAY、CURRENT CONSUMPTION OUT OF SPECIFICATION..... REJECTED	Critical
	13. PIN HOLE、PATTERN DEFORMITY	ACCORDING TO STANDARD OF VISUAL INSPECTION	Minor

8.4. STANDARD OF VISUAL INSPECTION

<table>
<tr><th>NO.</th><th>CLASS</th><th>ITEM</th><th>JUDGEMENT</th></tr>
<tr><td>8.4.1</td><td>MINOR</td><td>. BLEMISH、BLACK SPOT、WHITE SPOT IN THE LCD.

. BLEMISH、BLACK SPOT、WHITE SPOT AND SCRATCH ON THE POLARIZER</td><td>(A) ROUND TYPE: unit : mm.
<table>
<tr><th>DIAMETER (mm.)</th><th>ACCEPTABLE Q'TY</th></tr>
<tr><td>Φ ≦ 0.1</td><td>DISREGARD</td></tr>
<tr><td>0.1 < Φ ≦ 0.2</td><td>2</td></tr>
<tr><td>0.2 < Φ ≦ 0.25</td><td>1</td></tr>
<tr><td>0.25 < Φ</td><td>0</td></tr>
</table>
NOTE: Φ=(LENGTH+WIDTH)/2
(B) LINER TYPE: unit : mm.
<table>
<tr><th>LENGTH</th><th>WIDTH</th><th>ACCEPTABLE Q'TY</th></tr>
<tr><td>------</td><td>W ≦0.03</td><td>DISREGARD</td></tr>
<tr><td>L ≦ 5.0</td><td>0.03 < W ≦0.05</td><td>3</td></tr>
<tr><td>L ≦ 5.0</td><td>0.05 < W ≦0.07</td><td>1</td></tr>
<tr><td>------</td><td>0.07 < W</td><td>FOLLOW ROUND TYPE</td></tr>
</table></td></tr>
<tr><td>8.4.2</td><td>MINOR</td><td>BUBBLE IN POLARIZER</td><td>unit : mm.
<table>
<tr><th>DIAMETER</th><th>ACCEPTABLE Q'TY</th></tr>
<tr><td>Φ ≦0.15</td><td>DISREGARD</td></tr>
<tr><td>0.15 < Φ ≦ 0.5</td><td>2</td></tr>
<tr><td>0.5 < Φ</td><td>0</td></tr>
</table></td></tr>
<tr><td>8.4.3</td><td>MINOR</td><td>PIN HOLE 、PATTERN DEFORMITY</td><td> 

Φ=(a+b)/2
unit : mm.
<table>
<tr><th>DIAMETER</th><th>ACC. Q'TY</th></tr>
<tr><td>Φ ≦ 0.1</td><td>DISREGARD</td></tr>
<tr><td>0.1 < Φ ≦ 0.25</td><td>3</td></tr>
<tr><td>0.25 < Φ</td><td>0</td></tr>
</table></td></tr>
</table>

NO.	CLASS	ITEM	JUDGEMENT
8.4.4	MINOR	CHIPPING	 Y > S REJ.
8.4.5	MINOR	CHIPPING	 X or Y > S REJ.
8.4.6	MAJOR	GLASS CRACK	 Y > (1/2) T REJ.
8.4.7	MAJOR	SCRIBE DEFECT	 1. a> L/3 , A>1.5mm. REJ. 2. B : ACCORDING TO DIMENSION
8.4.8	MINOR	CHIPPING (ON THE TERMINAL AREA)	 Φ= (x+y)/2 > 2.5 mm REJ.
8.4.9	MINOR	CHIPPING (ON THE TERMINAL SURFACE)	 Y > (1/3) T REJ.
8.4.10	MINOR	CHIPPING	 Y > T REJ.