

MOSFET

Metal Oxide Semiconductor Field Effect Transistor

CoolMOS™ CE

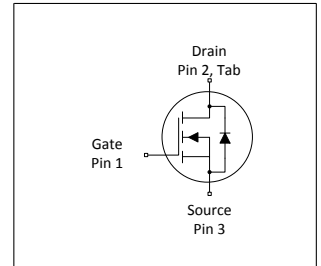
600V CoolMOS™ CE Power Transistor
IPx60R800CE

Data Sheet

Rev. 2.0
Final

1 Description

CoolMOS™ is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies. CoolMOS™ CE is a price-performance optimized platform enabling to target cost sensitive applications in Consumer and Lighting markets by still meeting highest efficiency standards. The new series provides all benefits of a fast switching Superjunction MOSFET while not sacrificing ease of use and offering the best cost down performance ratio available on the market.



Features

- Extremely low losses due to very low FOM $R_{DS(on)} \cdot Q_g$ and E_{oss}
- Very high commutation ruggedness
- Easy to use/drive
- Pb-free plating, Halogen free mold compound
- Qualified for consumer grade applications

Applications

PFC stages, hard switching PWM stages and resonant switching stages for e.g. PC Silverbox, Adapter, LCD & PDP TV and Lighting.

Please note: For MOSFET paralleling the use of ferrite beads on the gate or separate totem poles is generally recommended.



Table 1 Key Performance Parameters

Parameter	Value	Unit
$V_{DS} @ T_{j,max}$	650	V
$R_{DS(on),max}$	800	mΩ
$Q_{g,typ}$	17.2	nC
$I_{D,pulse}$	15.7	A
$E_{oss@400V}$	1.6	μJ
Body diode di/dt	500	A/μs

Type / Ordering Code	Package	Marking	Related Links
IPD60R800CE	PG-TO 252	6R800CE	see Appendix A
IPA60R800CE	PG-TO 220 FullPAK		

Table of Contents

Description	2
Maximum ratings	4
Thermal characteristics	5
Electrical characteristics	6
Electrical characteristics diagrams	8
Test Circuits	13
Package Outlines	14
Appendix A	16
Revision History	17
Disclaimer	17

2 Maximum ratings

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	5.6 3.5	A	$T_C=25^\circ\text{C}$ $T_C=100^\circ\text{C}$
Pulsed drain current ²⁾	$I_{D,pulse}$	-	-	15.7	A	$T_C=25^\circ\text{C}$
Avalanche energy, single pulse	E_{AS}	-	-	72	mJ	$I_D=1\text{A}$; $V_{DD}=50\text{V}$; see table 11
Avalanche energy, repetitive	E_{AR}	-	-	0.17	mJ	$I_D=1\text{A}$; $V_{DD}=50\text{V}$; see table 11
Avalanche current, repetitive	I_{AR}	-	-	1.0	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	50	V/ns	$V_{DS}=0\dots480\text{V}$
Gate source voltage (static)	V_{GS}	-20	-	20	V	static;
Gate source voltage (dynamic)	V_{GS}	-30	-	30	V	AC ($f>1\text{ Hz}$)
Power dissipation (Non FullPAK) TO-252	P_{tot}	-	-	48	W	$T_C=25^\circ\text{C}$
Power dissipation (FullPAK) TO-220FP	P_{tot}	-	-	27	W	$T_C=25^\circ\text{C}$
Storage temperature	T_{stg}	-40	-	150	$^\circ\text{C}$	-
Operating junction temperature	T_j	-40	-	150	$^\circ\text{C}$	-
Mounting torque (FullPAK) TO-220FP	-	-	-	50	Ncm	M2.5 screws
Continuous diode forward current	I_S	-	-	4.8	A	$T_C=25^\circ\text{C}$
Diode pulse current ²⁾	$I_{S,pulse}$	-	-	15.7	A	$T_C=25^\circ\text{C}$
Reverse diode dv/dt ³⁾	dv/dt	-	-	15	V/ns	$V_{DS}=0\dots400\text{V}$, $I_{SD}\leq I_S$, $T_j=25^\circ\text{C}$ see table 9
Maximum diode commutation speed	di_f/dt	-	-	500	A/ μs	$V_{DS}=0\dots400\text{V}$, $I_{SD}\leq I_S$, $T_j=25^\circ\text{C}$ see table 9
Insulation withstand voltage for TO-220FP	V_{ISO}	-	-	2500	V	V_{rms} , $T_C=25^\circ\text{C}$, $t=1\text{ min}$

¹⁾ Limited by $T_{j,max}$. Maximum duty cycle $D=0.75$

²⁾ Pulse width t_p limited by $T_{j,max}$

³⁾ Identical low side and high side switch with identical R_G

3 Thermal characteristics

Table 3 Thermal characteristics (FullPAK) TO-220FP

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	4.6	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	80	°C/W	leaded
Soldering temperature, wavesoldering only allowed at leads	T_{sold}	-	-	260	°C	1.6mm (0.063 in.) from case for 10s

Table 4 Thermal characteristics TO-252

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	2.6	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	62	°C/W	device on PCB, minimal footprint
Thermal resistance, junction - ambient for SMD version	R_{thJA}	-	35	45	°C/W	Device on 40mm*40mm*1.5mm epoxy PCB FR4 with 6cm ² (one layer, 70μm thickness) copper area for drain connection and cooling. PCB is vertical without air stream cooling.
Soldering temperature, wave & reflow soldering allowed	T_{sold}	-	-	260	°C	reflow MSL1

4 Electrical characteristics

at $T_j=25^\circ\text{C}$, unless otherwise specified

Table 5 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	600	-	-	V	$V_{GS}=0\text{V}$, $I_D=0.25\text{mA}$
Gate threshold voltage	$V_{(GS)th}$	2.5	3.0	3.5	V	$V_{DS}=V_{GS}$, $I_D=0.17\text{mA}$
Zero gate voltage drain current	I_{DSS}	-	-	1	μA	$V_{DS}=600$, $V_{GS}=0\text{V}$, $T_j=25^\circ\text{C}$ $V_{DS}=600$, $V_{GS}=0\text{V}$, $T_j=150^\circ\text{C}$
Gate-source leakage current	I_{GSS}	-	-	100	nA	$V_{GS}=20\text{V}$, $V_{DS}=0\text{V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	0.68 1.76	0.80 -	Ω	$V_{GS}=10\text{V}$, $I_D=2\text{A}$, $T_j=25^\circ\text{C}$ $V_{GS}=10\text{V}$, $I_D=2\text{A}$, $T_j=150^\circ\text{C}$
Gate resistance	R_G	-	11	-	Ω	$f=1\text{MHz}$, open drain

Table 6 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	373	-	pF	$V_{GS}=0\text{V}$, $V_{DS}=100\text{V}$, $f=1\text{MHz}$
Output capacitance	C_{oss}	-	27	-	pF	$V_{GS}=0\text{V}$, $V_{DS}=100\text{V}$, $f=1\text{MHz}$
Effective output capacitance, energy related ¹⁾	$C_{o(er)}$	-	18	-	pF	$V_{GS}=0\text{V}$, $V_{DS}=0\dots480\text{V}$
Effective output capacitance, time related ²⁾	$C_{o(tr)}$	-	74	-	pF	$I_D=\text{constant}$, $V_{GS}=0\text{V}$, $V_{DS}=0\dots480\text{V}$
Turn-on delay time	$t_{d(on)}$	-	9	-	ns	$V_{DD}=400\text{V}$, $V_{GS}=13\text{V}$, $I_D=2.5\text{A}$, $R_G=6.8\Omega$; see table 10
Rise time	t_r	-	7	-	ns	$V_{DD}=400\text{V}$, $V_{GS}=13\text{V}$, $I_D=2.5\text{A}$, $R_G=6.8\Omega$; see table 10
Turn-off delay time	$t_{d(off)}$	-	50	-	ns	$V_{DD}=400\text{V}$, $V_{GS}=13\text{V}$, $I_D=2.5\text{A}$, $R_G=6.8\Omega$; see table 10
Fall time	t_f	-	12	-	ns	$V_{DD}=400\text{V}$, $V_{GS}=13\text{V}$, $I_D=2.5\text{A}$, $R_G=6.8\Omega$; see table 10

Table 7 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	2	-	nC	$V_{DD}=480\text{V}$, $I_D=2.5\text{A}$, $V_{GS}=0$ to 10V
Gate to drain charge	Q_{gd}	-	8.9	-	nC	$V_{DD}=480\text{V}$, $I_D=2.5\text{A}$, $V_{GS}=0$ to 10V
Gate charge total	Q_g	-	17.2	-	nC	$V_{DD}=480\text{V}$, $I_D=2.5\text{A}$, $V_{GS}=0$ to 10V
Gate plateau voltage	$V_{plateau}$	-	5.4	-	V	$V_{DD}=480\text{V}$, $I_D=2.5\text{A}$, $V_{GS}=0$ to 10V

¹⁾ $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% $V_{(BR)DSS}$

²⁾ $C_{o(tr)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% $V_{(BR)DSS}$

Table 8 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	0.9	-	V	$V_{GS}=0V, I_F=2.5A, T_j=25^\circ C$
Reverse recovery time	t_{rr}	-	250	-	ns	$V_R=400V, I_F=2.5A, di_F/dt=100A/\mu s$; see table 9
Reverse recovery charge	Q_{rr}	-	1.8	-	μC	$V_R=400V, I_F=2.5A, di_F/dt=100A/\mu s$; see table 9
Peak reverse recovery current	I_{rrm}	-	16	-	A	$V_R=400V, I_F=2.5A, di_F/dt=100A/\mu s$; see table 9

5 Electrical characteristics diagrams

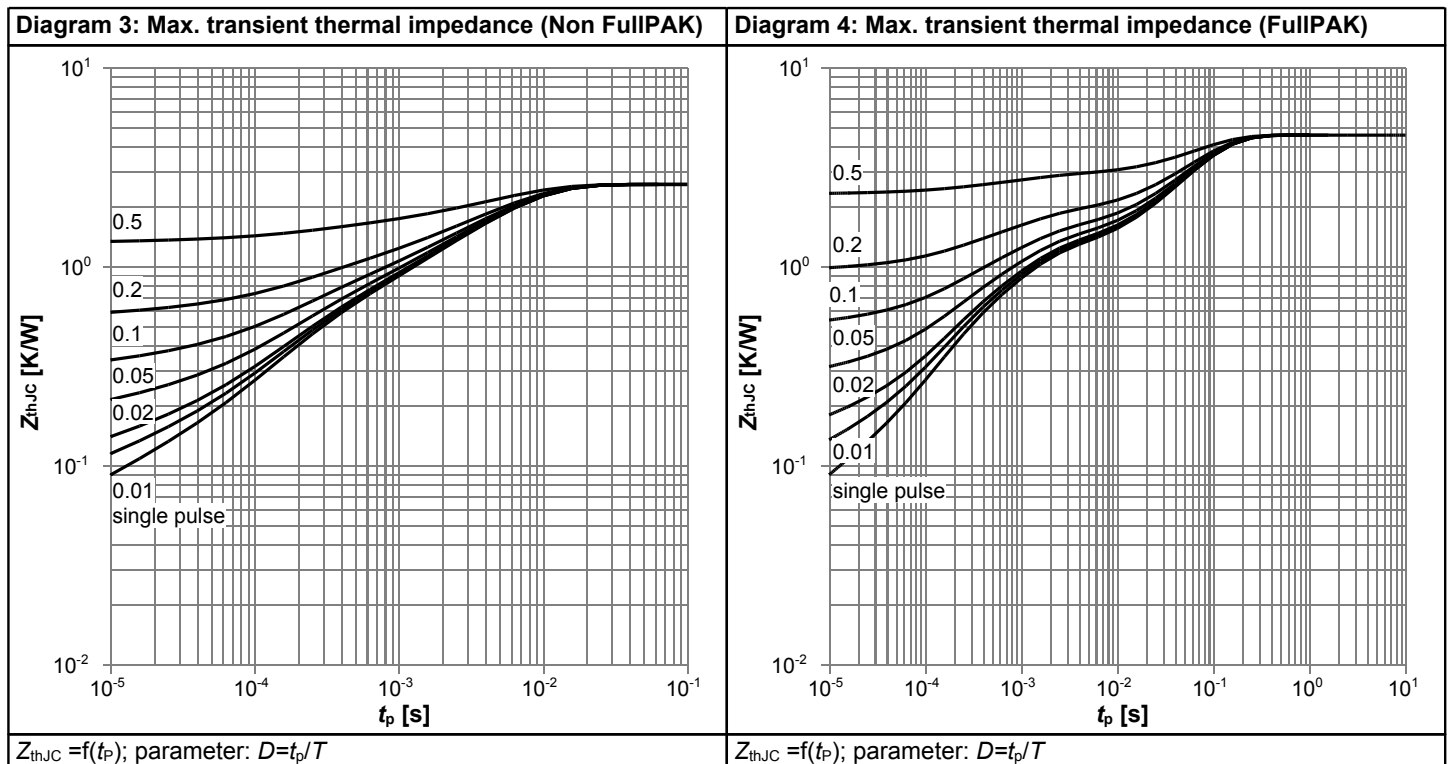
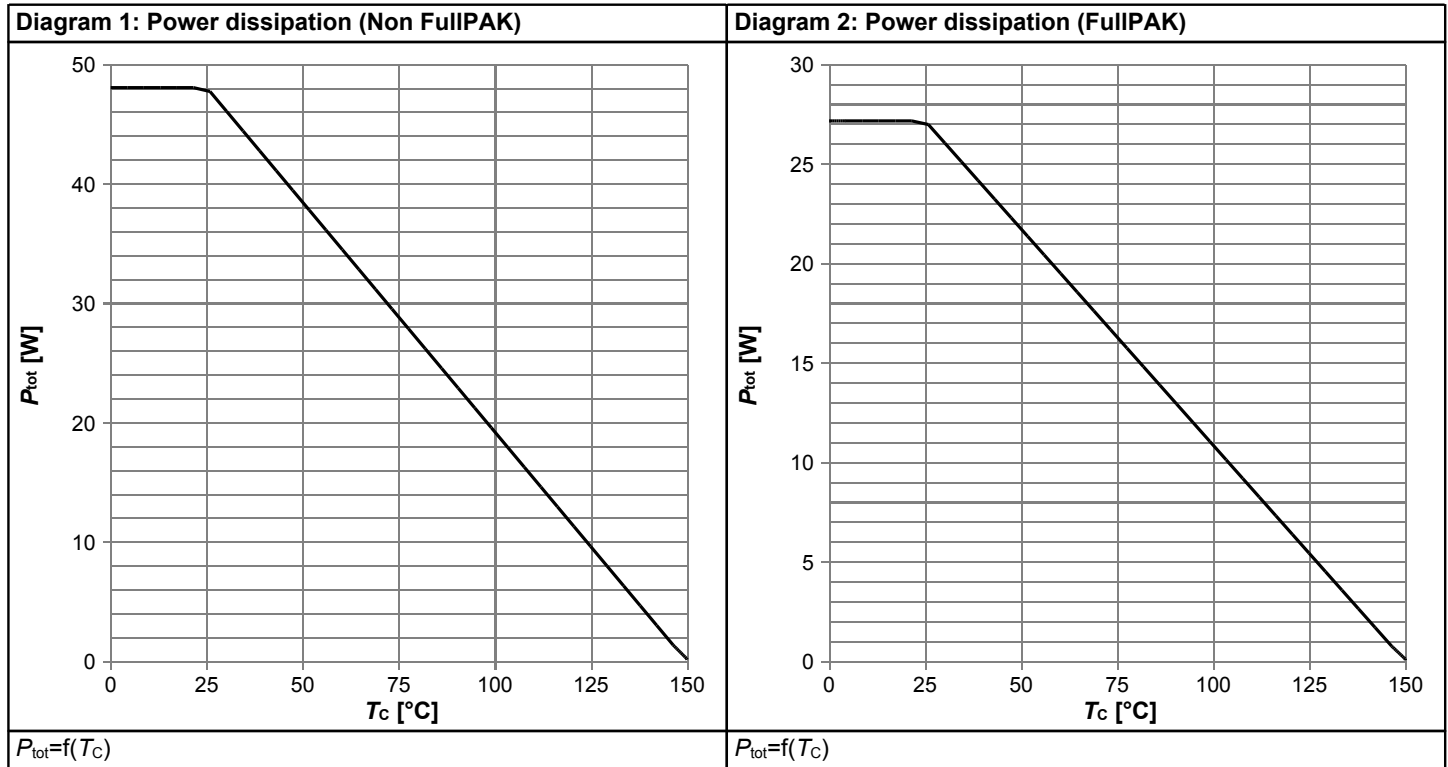
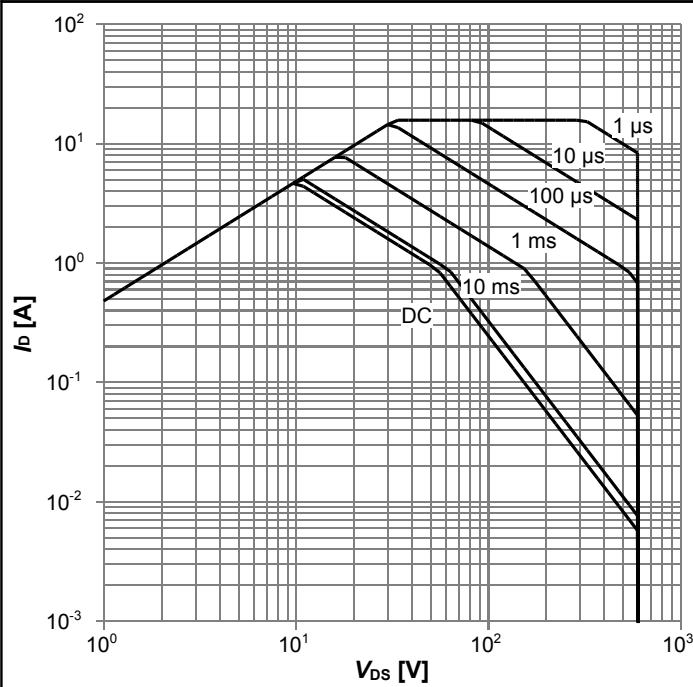
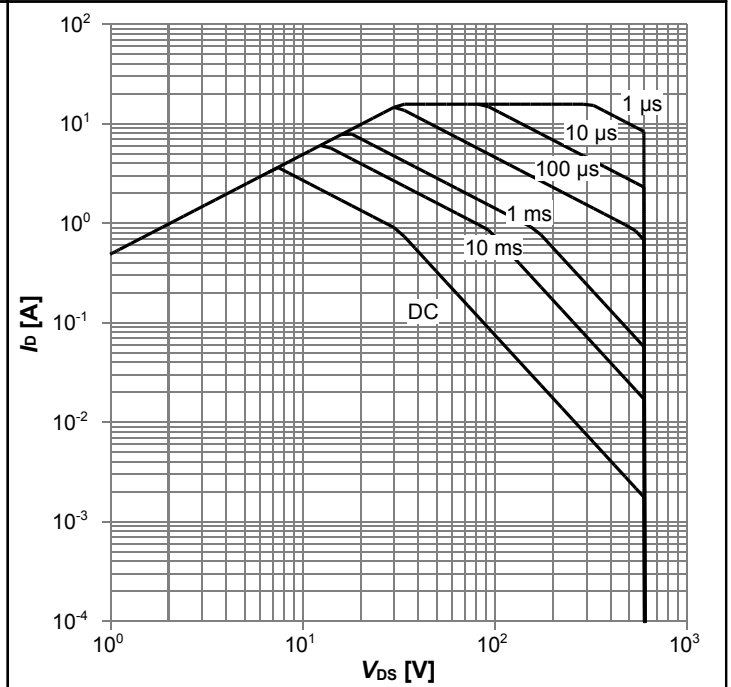


Diagram 5: Safe operating area (Non FullPAK)



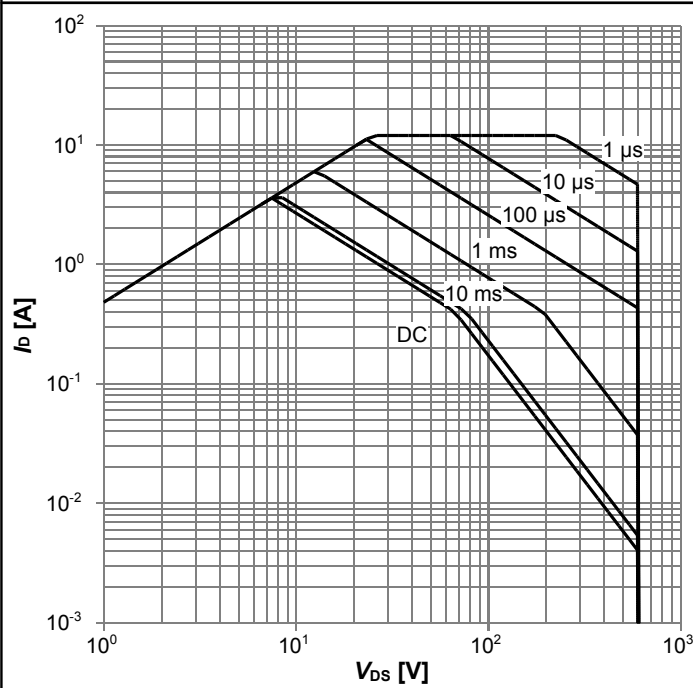
$I_D=f(V_{DS}); T_C=25\text{ }^\circ\text{C}; D=0$; parameter: t_p

Diagram 6: Safe operating area (FullPAK)



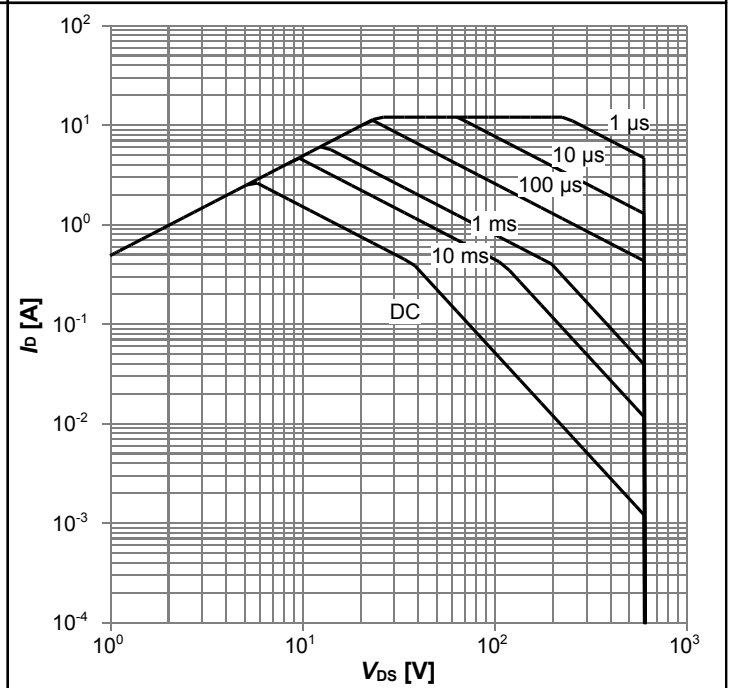
$I_D=f(V_{DS}); T_C=25\text{ }^\circ\text{C}; D=0$; parameter: t_p

Diagram 7: Safe operating area (Non FullPAK)



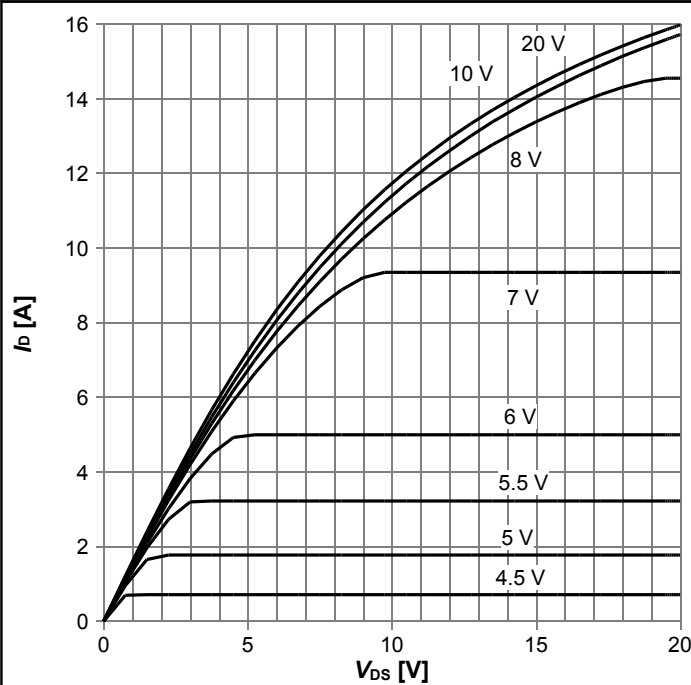
$I_D=f(V_{DS}); T_C=80\text{ }^\circ\text{C}; D=0$; parameter: t_p

Diagram 8: Safe operating area (FullPAK)



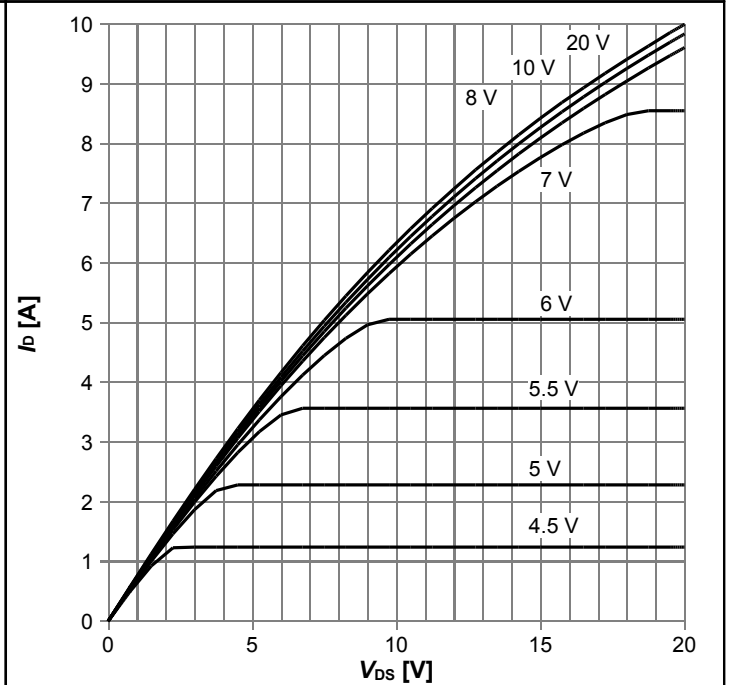
$I_D=f(V_{DS}); T_C=80\text{ }^\circ\text{C}; D=0$; parameter: t_p

Diagram 9: Typ. output characteristics



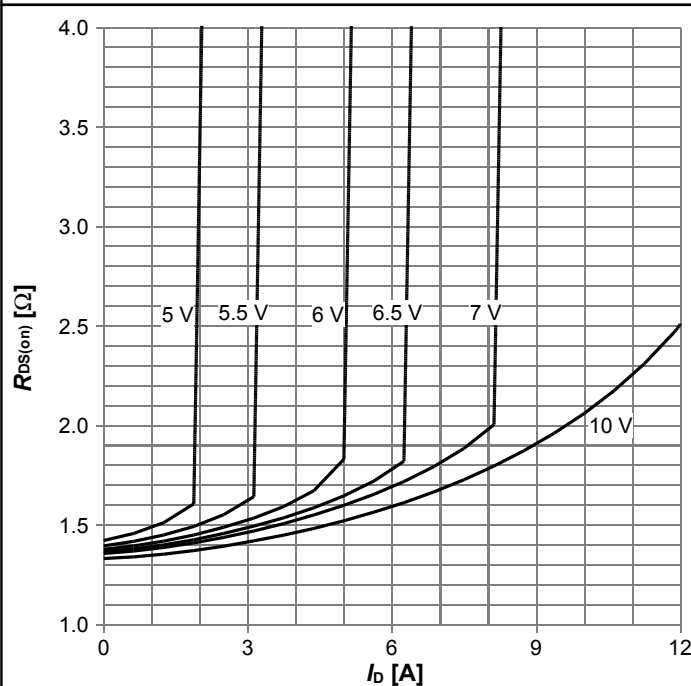
$I_D = f(V_{DS})$; $T_j = 25^\circ\text{C}$; parameter: V_{GS}

Diagram 10: Typ. output characteristics



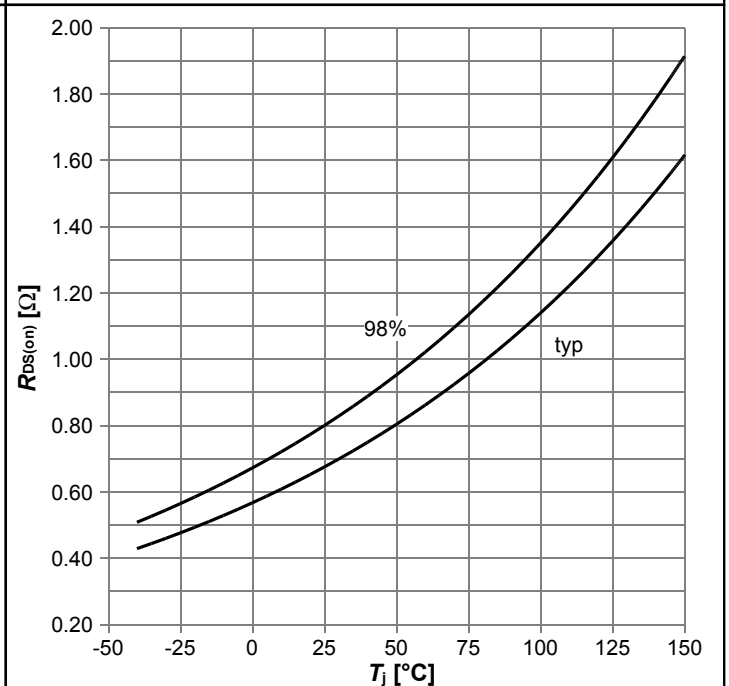
$I_D = f(V_{DS})$; $T_j = 125^\circ\text{C}$; parameter: V_{GS}

Diagram 11: Typ. drain-source on-state resistance



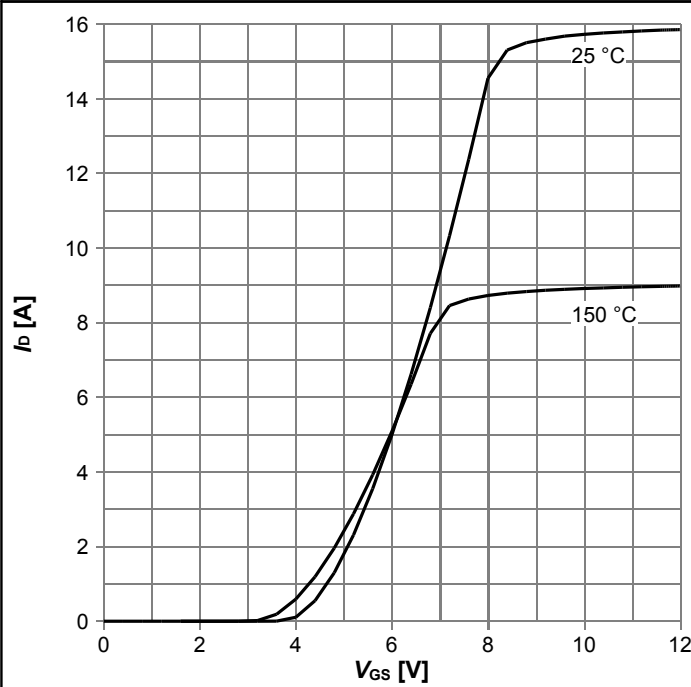
$R_{DS(on)} = f(I_D)$; $T_j = 125^\circ\text{C}$; parameter: V_{GS}

Diagram 12: Drain-source on-state resistance



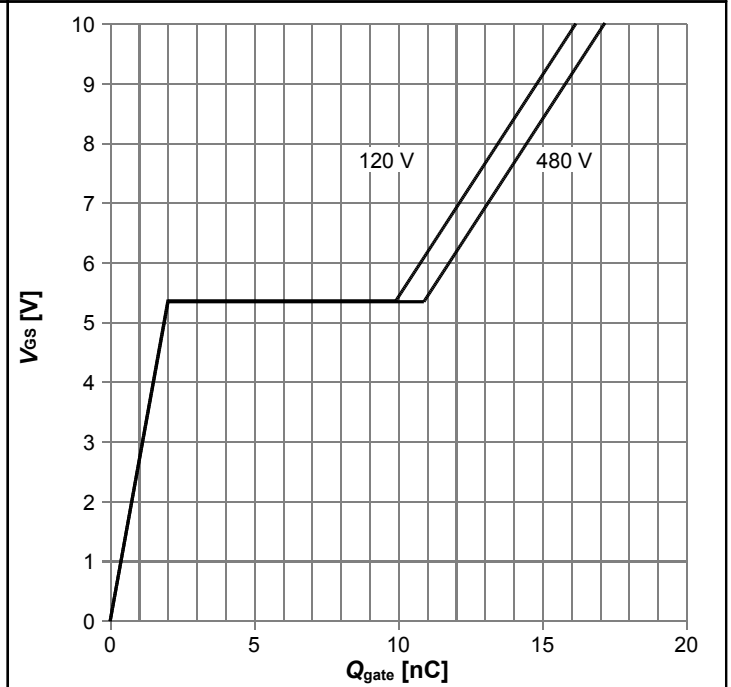
$R_{DS(on)} = f(T_j)$; $I_D = 2.0\text{ A}$; $V_{GS} = 10\text{ V}$

Diagram 13: Typ. transfer characteristics



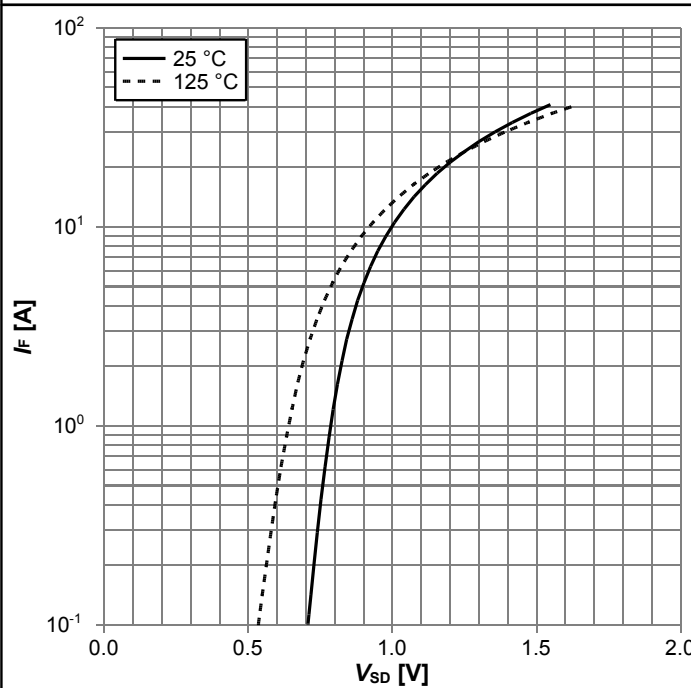
$I_D=f(V_{GS}); V_{DS}=20V; \text{parameter: } T_j$

Diagram 14: Typ. gate charge



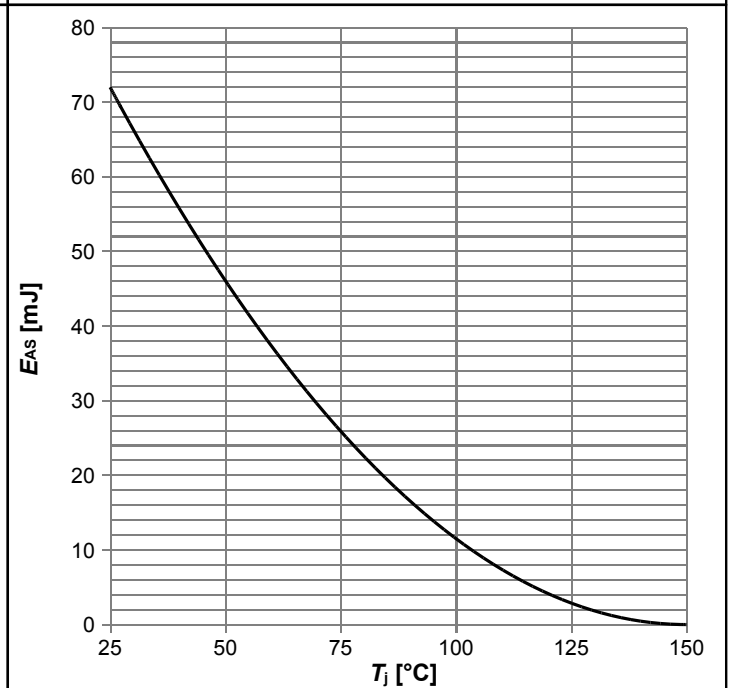
$V_{GS}=f(Q_{gate}); I_D=2.5 \text{ A pulsed}; \text{parameter: } V_{DD}$

Diagram 15: Forward characteristics of reverse diode



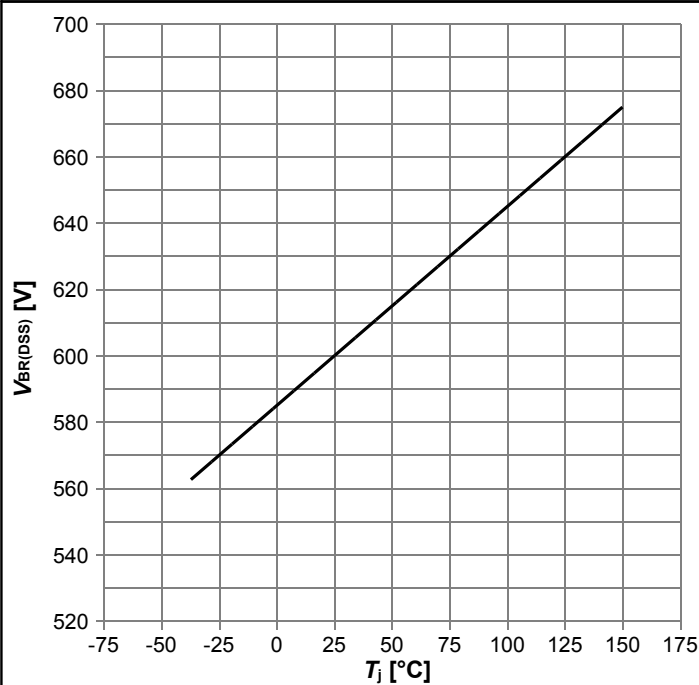
$I_F=f(V_{SD}); \text{parameter: } T_j$

Diagram 16: Avalanche energy



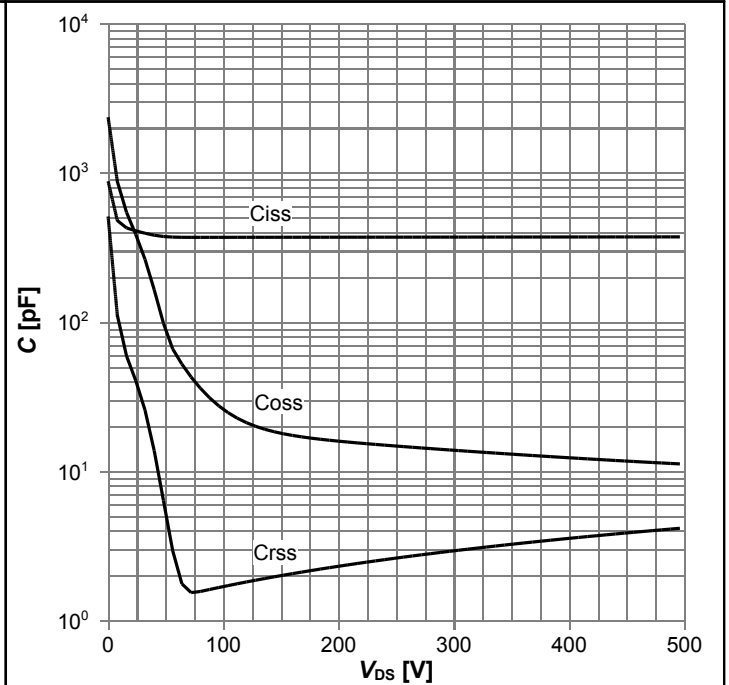
$E_{AS}=f(T_j); I_D=1.0 \text{ A}; V_{DD}=50 \text{ V}$

Diagram 17: Drain-source breakdown voltage



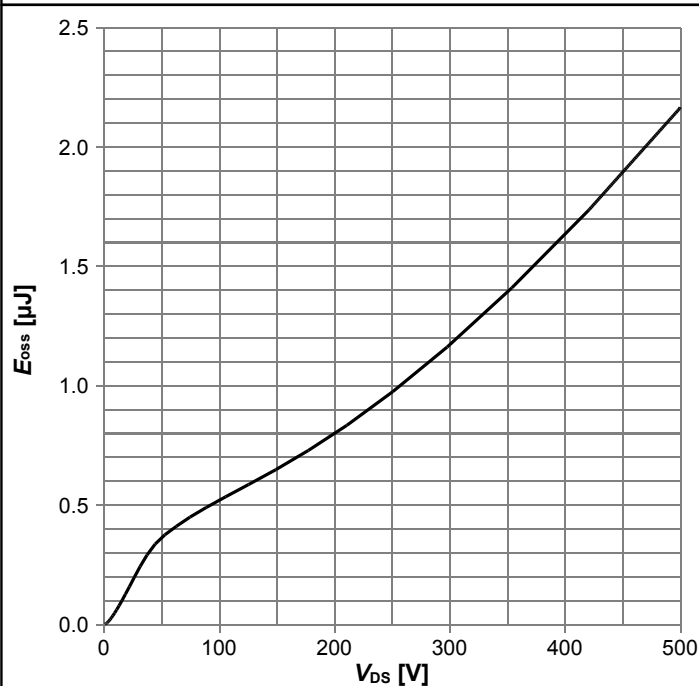
$V_{BR(DSS)}=f(T_j); I_D=0.25 \text{ mA}$

Diagram 18: Typ. capacitances



$C=f(V_{DS}); V_{GS}=0 \text{ V}; f=1 \text{ MHz}$

Diagram 19: Typ. Coss stored energy



$E_{oss}=f(V_{DS})$

6 Test Circuits

Table 9 Diode characteristics

Test circuit for diode characteristics	Diode recovery waveform
<p>$R_{g1} = R_{g2}$</p>	<p> $t_{rr} = t_F + t_S$ $Q_r = Q_F + Q_S$ </p>

Table 10 Switching times

Switching times test circuit for inductive load	Switching times waveform

Table 11 Unclamped inductive load

Unclamped inductive load test circuit	Unclamped inductive waveform

7 Package Outlines

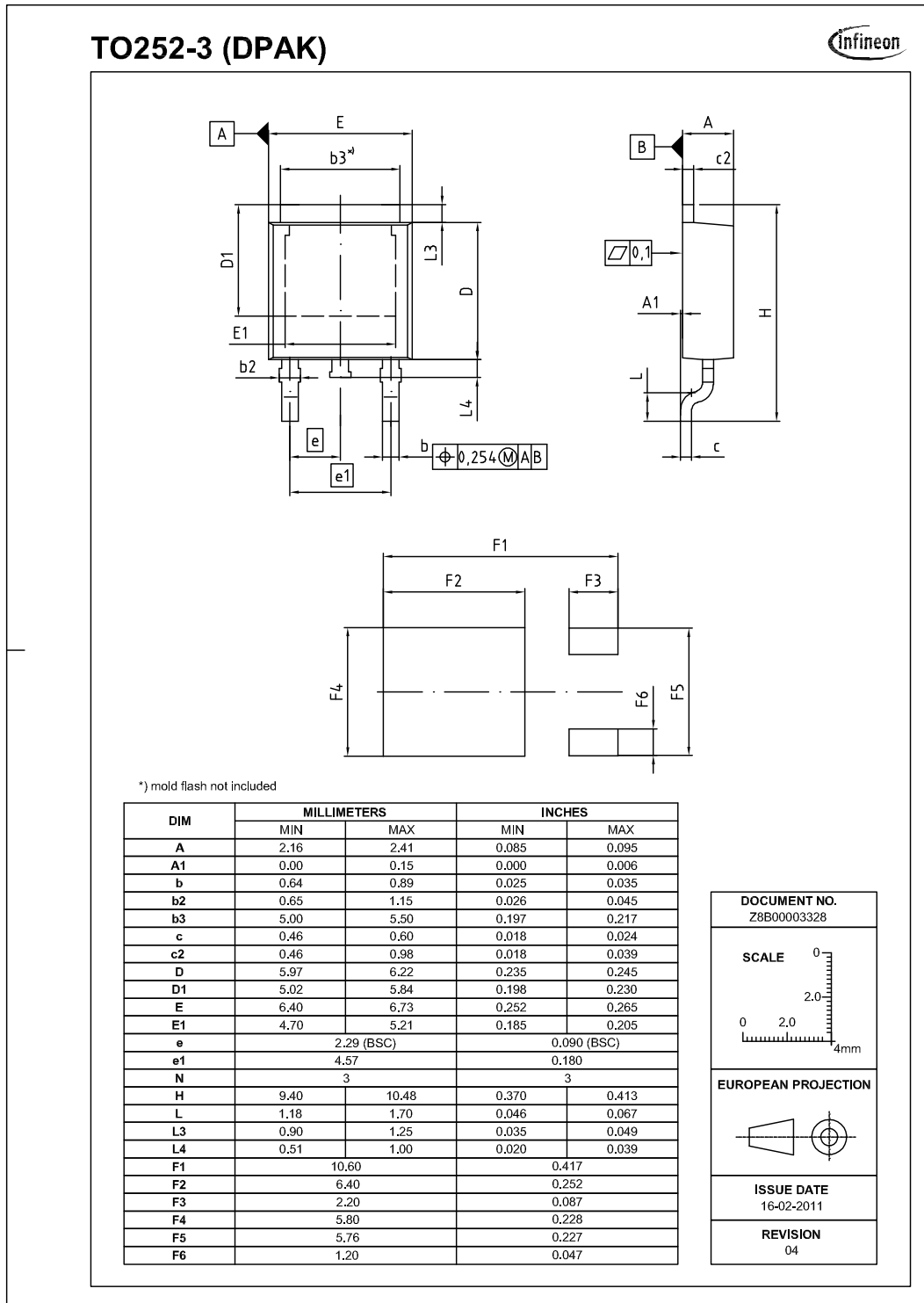
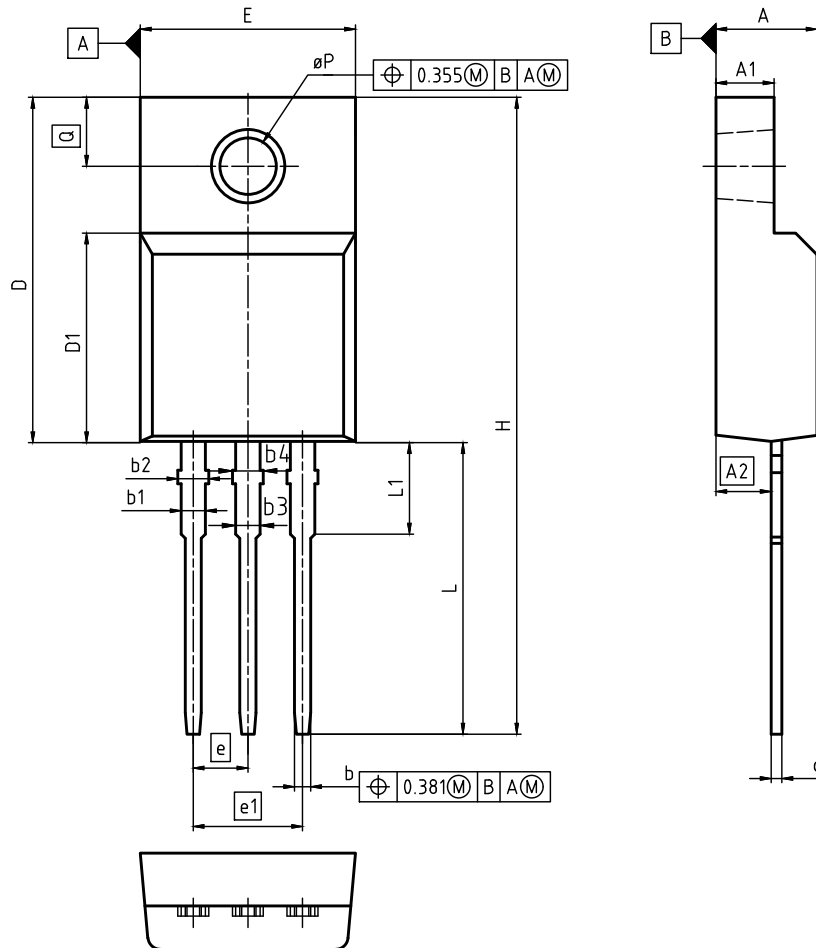


Figure 1 Outline PG-TO 252, dimensions in mm/inches



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.50	4.90	0.177	0.193
A1	2.34	2.85	0.092	0.112
A2	2.42	2.86	0.095	0.113
b	0.65	0.90	0.026	0.035
b1	0.95	1.38	0.037	0.054
b2	0.95	1.51	0.037	0.059
b3	0.65	1.38	0.026	0.054
b4	0.65	1.51	0.026	0.059
c	0.40	0.63	0.016	0.025
D	15.67	16.15	0.617	0.636
D1	8.97	9.83	0.353	0.387
E	10.00	10.65	0.394	0.419
e	2.54 (BSC)		0.100 (BSC)	
e1	5.08		0.200	
N	3		3	
H	28.70	29.75	1.130	1.171
L	12.78	13.75	0.503	0.541
L1	2.83	3.45	0.111	0.136
øP	2.95	3.38	0.116	0.133
Q	3.15	3.50	0.124	0.138

DOCUMENT NO.
Z8B00003319

SCALE

EUROPEAN PROJECTION

ISSUE DATE
05-05-2014

REVISION
04

Dimensions do not include mold flash, protrusions or gate burrs

Figure 2 Outline PG-TO 220 FullPAK, dimensions in mm/inches

8 Appendix A

Table 12 Related Links

- IFX CoolMOS™ CE Webpage: www.infineon.com
- IFX CoolMOS™ CE application note: www.infineon.com
- IFX CoolMOS™ CE simulation model: www.infineon.com
- IFX Design tools: www.infineon.com

Revision History

IPD60R800CE, IPA60R800CE

Revision: 2014-09-25, Rev. 2.0

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2014-09-25	Release of final version

We Listen to Your Comments

Any information within this document that you feel is wrong, unclear or missing at all? Your feedback will help us to continuously improve the quality of this document. Please send your proposal (including a reference to this document) to: erratum@infineon.com

Published by

Infineon Technologies AG
81726 München, Germany
© 2014 Infineon Technologies AG
All Rights Reserved.

Legal Disclaimer

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation, warranties of non-infringement of intellectual property rights of any third party.

Information

For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office (www.infineon.com).

Warnings

Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.

The Infineon Technologies component described in this Data Sheet may be used in life-support devices or systems and/or automotive, aviation and aerospace applications or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support, automotive, aviation and aerospace device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.