ICM-20602

High Performance 6-Axis MEMS MotionTracking™ Device

General Description

The ICM-20602 is a 6-axis MotionTracking device that combines a 3-axis gyroscope, 3-axis accelerometer, in a small 3 mm x 3 mm x 0.75 mm (16-pin LGA) package.

- High performance specs
  - Gyroscope sensitivity error: ±1%
  - Gyroscope noise: ±4 mdps/√Hz
  - Accelerometer noise: 100 µg/√Hz
- Includes 1 KB FIFO to reduce traffic on the serial bus interface, and reduce power consumption by allowing the system processor to burst read sensor data and then go into a low-power mode
- EIS FSYNC support

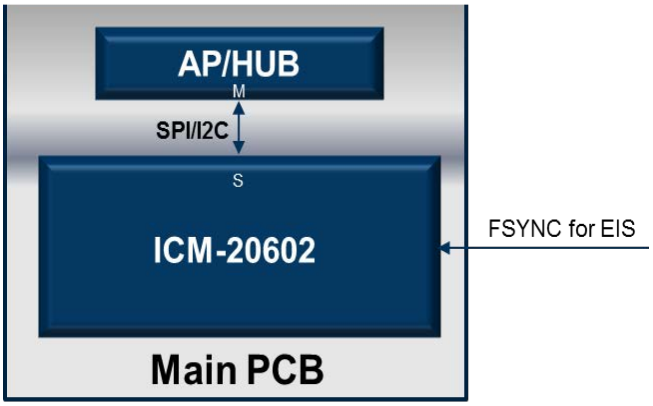
ICM-20602 includes on-chip 16-bit ADCs, programmable digital filters, an embedded temperature sensor, and programmable interrupts. The device features an operating voltage range down to 1.71V. Communication ports include I^2C and high speed SPI at 10 MHz.

Ordering Information

PART	TEMP RANGE	PACKAGE
ICM-20602†	–40°C to +85°C	16-Pin LGA

†Denotes RoHS and Green-Compliant Package

Block Diagram



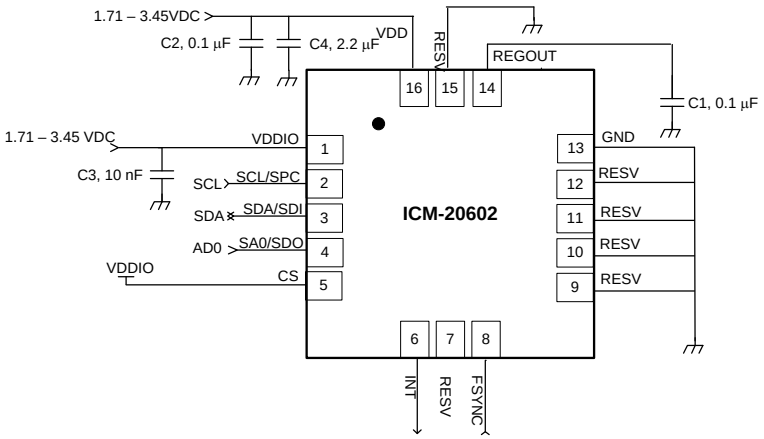
Applications

- Smartphones and Tablets
- Wearable Sensors
- IoT Applications
- Motion-based game controllers
- 3D remote controls for Internet connected DTVs and set top boxes, 3D mice

Features

- 3-Axis Gyroscope with Programmable FSR of ±250 dps, ±500 dps, ±1000 dps, and ±2000 dps
- 3-Axis Accelerometer with Programmable FSR of ±2*g*, ±4*g*, ±8*g*, and ±16*g*
- User-programmable interrupts
- Wake-on-motion interrupt for low power operation of applications processor
- 1 KB FIFO buffer enables the applications processor to read the data in bursts
- On-Chip 16-bit ADCs and Programmable Filters
- Host interface: 10 MHz SPI or 400 kHz Fast Mode I^2C
- Digital-output temperature sensor
- VDD operating range of 1.71V to 3.45V
- MEMS structure hermetically sealed and bonded at wafer level
- RoHS and Green compliant

Typical Operating Circuit



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1 INTRODUCTION

1.1 PURPOSE AND SCOPE

This document is a product specification, providing a description, specifications, and design related information on the ICM-20602™ MotionTracking device. The device is housed in a small 3 mm x 3 mm x 0.75 mm 16-pin LGA package.

1.2 PRODUCT OVERVIEW

The ICM-20602 is a 6-axis MotionTracking device that combines a 3-axis gyroscope, 3-axis accelerometer, in a small 3 mm x 3 mm x 0.75 mm (16-pin LGA) package. It also features a 1 KB FIFO that can lower the traffic on the serial bus interface, and reduce power consumption by allowing the system processor to burst read sensor data and then go into a low-power mode. ICM-20602, with its 6-axis integration, enables manufacturers to eliminate the costly and complex selection, qualification, and system level integration of discrete devices, guaranteeing optimal motion performance for consumers.

The gyroscope has a programmable full-scale range of ±250 dps, ±500 dps, ±1000 dps, and ±2000 dps. The accelerometer has a user-programmable accelerometer full-scale range of ±2*g*, ±4*g*, ±8*g*, and ±16*g*. Factory-calibrated initial sensitivity of both sensors reduces production-line calibration requirements.

Other industry-leading features include on-chip 16-bit ADCs, programmable digital filters, an embedded temperature sensor, and programmable interrupts. The device features I^2C and SPI serial interfaces, a VDD operating range of 1.71V to 3.45V, and a separate digital IO supply, VDDIO from 1.71V to 3.45V.

Communication with all registers of the device is performed using either I^2C at 400 kHz or SPI at 10 MHz.

By leveraging its patented and volume-proven CMOS-MEMS fabrication platform, which integrates MEMS wafers with companion CMOS electronics through wafer-level bonding, TDK-InvenSense has driven the package size down to a footprint and thickness of 3 mm x 3 mm x 0.75 mm (16-pin LGA), to provide a very small yet high performance, low cost package. The device provides high robustness by supporting 20,000*g* shock reliability.

1.3 APPLICATIONS

- Smartphones and Tablets
- Wearable Sensors

2 FEATURES

2.1 GYROSCOPE FEATURES

The triple-axis MEMS gyroscope in the ICM-20602 includes a wide range of features:

- Digital-output X-, Y-, and Z-axis angular rate sensors (gyroscopes) with a user-programmable full-scale range of ±250 dps, ±500 dps, ±1000 dps, and ±2000 dps and integrated 16-bit ADCs
- Digitally-programmable low-pass filter
- Low-power gyroscope operation
- Factory calibrated sensitivity scale factor
- Self-test

2.2 ACCELEROMETER FEATURES

The triple-axis MEMS accelerometer in ICM-20602 includes a wide range of features:

- Digital-output X-, Y-, and Z-axis accelerometer with a programmable full-scale range of ±2*g*, ±4*g*, ±8*g*, and ±16*g* and integrated 16-bit ADCs
- User-programmable interrupts
- Wake-on-motion interrupt for low power operation of applications processor
- Self-test

2.3 ADDITIONAL FEATURES

The ICM-20602 includes the following additional features:

- Smallest and thinnest LGA package for portable devices: 3 mm x 3 mm x 0.75 mm (16-pin LGA)
- Minimal cross-axis sensitivity between the accelerometer and gyroscope axes
- 1 KB FIFO buffer enables the applications processor to read the data in bursts
- Digital-output temperature sensor
- User-programmable digital filters for gyroscope, accelerometer, and temp sensor
- 20,000 *g* shock tolerant
- 400 kHz Fast Mode I^2C for communicating with all registers
- 10 MHz SPI serial interface for communicating with all registers
- MEMS structure hermetically sealed and bonded at wafer level
- RoHS and Green compliant

3 ELECTRICAL CHARACTERISTICS

3.1 GYROSCOPE SPECIFICATIONS

Typical Operating Circuit of section 4.2, VDD = 1.8V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
GYROSCOPE SENSITIVITY						
Full-Scale Range	FS_SEL=0		±250		dps	3
	FS_SEL=1		±500		dps	3
	FS_SEL=2		±1000		dps	3
	FS_SEL=3		±2000		dps	3
Gyroscope ADC Word Length			16		bits	3
Sensitivity Scale Factor	FS_SEL=0		131		LSB/(dps)	3
	FS_SEL=1		65.5		LSB/(dps)	3
	FS_SEL=2		32.8		LSB/(dps)	3
	FS_SEL=3		16.4		LSB/(dps)	3
Sensitivity Scale Factor Initial Tolerance	25°C		±1		%	1
Sensitivity Scale Factor Variation Over Temperature	-40°C to +85°C		±2		%	1
Nonlinearity	Best fit straight line; 25°C		±0.1		%	1
Cross-Axis Sensitivity			±1		%	1
ZERO-RATE OUTPUT (ZRO)						
Initial ZRO Tolerance	25°C		±1		dps	1
ZRO Variation vs. Temperature	-40°C to +85°C		±0.01		dps/ºC	1
OTHER PARAMETERS						
Rate Noise Spectral Density	@ 10 Hz		0.004		dps /√Hz	1, 4
Total RMS Noise	Bandwidth = 100 Hz		0.04		dps -rms	1, 4
Gyroscope Mechanical Frequencies		25	27	29	KHz	2
Low Pass Filter Response	Programmable Range	5		250	Hz	3
Gyroscope Start-Up Time	Time from gyro enable to gyro drive ready		35	100	ms	1
Output Data Rate	Low-Noise mode	3.91		8000	Hz	3
	Low Power Mode	3.91		333.33	Hz	3

Table 1. Gyroscope Specifications

Notes:

1. Derived from validation or characterization of parts, not guaranteed in production.
2. Tested in production.
3. Guaranteed by design.
4. Noise specifications shown are for low-noise mode.

3.2 ACCELEROMETER SPECIFICATIONS

Typical Operating Circuit of section 4.2, VDD = 1.8V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS	NOTES
ACCELEROMETER SENSITIVITY							
Full-Scale Range	AFS_SEL=0			±2		*g*	2
	AFS_SEL=1			±4		*g*	2
	AFS_SEL=2			±8		*g*	2
	AFS_SEL=3			±16		*g*	2
ADC Word Length	Output in two's complement format			16		bits	2
Sensitivity Scale Factor	AFS_SEL=0			16,384		LSB/*g*	2
	AFS_SEL=1			8,192		LSB/*g*	2
	AFS_SEL=2			4,096		LSB/*g*	2
	AFS_SEL=3			2,048		LSB/*g*	2
Sensitivity Scale Factor Initial Tolerance	Component-level			±1		%	1
Sensitivity Change vs. Temperature	-40°C to +85°C			±1.5		%	1
Nonlinearity	Best Fit Straight Line			±0.3		%	1
Cross-Axis Sensitivity				±1		%	1
ZERO-G OUTPUT							
Initial Tolerance	Component-level, all axes			±25		m*g*	1
	Board-level, all axes			±40		m*g*	1
Zero-G Level Change vs. Temperature	-40°C to +85°C	X and Y axes		±0.5		m*g*/ºC	1
		Z axis		±1		m*g*/ºC	1
OTHER PARAMETERS							
Power Spectral Density	@ 10 Hz			100		µg/√Hz	1, 3
RMS Noise	Bandwidth = 100 Hz			1.0		mg-rms	1, 3
Low-Pass Filter Response	Programmable Range		5		218	Hz	2
Accelerometer Startup Time	From sleep mode to valid data			10	20	ms	2
Output Data Rate	Low-Noise mode		3.91		4000	Hz	2
	Low Power Mode		3.91		500	Hz	

Table 2. Accelerometer Specifications

Notes:

1. Derived from validation or characterization of parts, not guaranteed in production.
2. Guaranteed by design.
3. Noise specifications shown are for low-noise mode.

3.3 ELECTRICAL SPECIFICATIONS

D.C. Electrical Characteristics

Typical Operating Circuit of section 4.2, VDD = 1.8V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
SUPPLY VOLTAGES						
VDD		1.71	1.8	3.45	V	1
VDDIO		1.71	1.8	3.45	V	1
SUPPLY CURRENTS						
Low-Noise Mode	6-Axis Gyroscope + Accelerometer		2.79		mA	1
	3-Axis Accelerometer		321		µA	1
	3-Axis Gyroscope		2.55		mA	1
Accelerometer Low -Power Mode (Gyroscope disabled)	100 Hz ODR, 1x averaging		40		µA	1
Gyroscope Low-Power Mode (Accelerometer disabled)	100 Hz ODR, 1x averaging		1.08		mA	1
6-Axis Low-Power Mode (Gyroscope Low-Power Mode; Accelerometer Low-Noise Mode)	100 Hz ODR, 1x averaging		1.33		mA	1
Full-Chip Sleep Mode	At 25ºC		6		µA	1
Specified Temperature Range	Performance parameters are not applicable beyond Specified Temperature Range	-40		+85	°C	1

Table 3. D.C. Electrical Characteristics

Notes:

1. Derived from validation or characterization of parts, not guaranteed in production.

A.C. Electrical Characteristics

Typical Operating Circuit of section 4.2, VDD = 1.8V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
SUPPLIES						
Supply Ramp Time	Monotonic ramp. Ramp rate is 10% to 90% of the final value	0.01		3	ms	1
Power Supply Noise			10		mV peak-peak	1
TEMPERATURE SENSOR						
Operating Range	Ambient	-40		85	°C	1
25°C Output			0		LSB	3
ADC Resolution			16		bits	2
ODR	Without Filter		8000		Hz	2
	With Filter	3.91		1000	Hz	2
Room Temperature Offset	25°C	-15		15	°C	3
Stabilization Time				14000	µs	2
Sensitivity	Untrimmed		326.8		LSB/°C	1
Sensitivity Error		-2.5		+2.5	%	1
Power-On RESET						
Start-up time for register read/write	From power-up			2	ms	1
I²C ADDRESS						
I²C ADDRESS	SA0 = 0 SA0 = 1		1101000 1101001			
DIGITAL INPUTS (FSYNC, SA0, SPC, SDI, CS)						
V_{IH}, High Level Input Voltage		0.7*VDDIO			V	1
V_{IL}, Low Level Input Voltage				0.3*VDDIO	V	
C_I, Input Capacitance			< 10		pF	
DIGITAL OUTPUT (SDO, INT, DRDY)						
V_{OH}, High Level Output Voltage	R_{LOAD}=1MΩ;	0.9*VDDIO			V	1
V_{OL1}, LOW-Level Output Voltage	R_{LOAD}=1MΩ;			0.1*VDDIO	V	
$V_{OL.INT}$, INT Low-Level Output Voltage	OPEN=1, 0.3mA sink Current			0.1	V	
Output Leakage Current	OPEN=1		100		nA	
t_{INT}, INT Pulse Width	LATCH_INT_EN=0		50		µs	
I²C I/O (SCL, SDA)						
V_{IL}, LOW Level Input Voltage		-0.5V		0.3*VDDIO	V	1
V_{IH}, HIGH-Level Input Voltage		0.7*VDDIO		VDDIO + 0.5V	V	
V_{hys}, Hysteresis			0.1*VDDIO		V	
V_{OL}, LOW-Level Output Voltage	3mA sink current	0		0.4	V	
I_{OL}, LOW-Level Output Current	V_{OL}=0.4V V_{OL}=0.6V		3 6		mA mA	
Output Leakage Current			100		nA	
t_{of}, Output Fall Time from V_{IHmax} to V_{ILmax}	C_b bus capacitance in pf	20+0.1C_b		300	ns	
INTERNAL CLOCK SOURCE						
Sample Rate	FCHOICE_B=1,2,3; SMPLRT_DIV=0		32		kHz	2
	FCHOICE_B=0; DLPFCFG=0 or 7 SMPLRT_DIV=0		8		kHz	2
	FCHOICE_B=0; DLPFCFG=1,2,3,4,5,6; SMPLRT_DIV=0		1		kHz	2
Clock Frequency Initial Tolerance	CLK_SEL=0, 6 or gyro inactive; 25°C	-3		+3	%	1
	CLK_SEL=1,2,3,4,5 and gyro active; 25°C	-1		+1	%	1
Frequency Variation over Temperature	CLK_SEL=0,6 or gyro inactive. (-40°C to +85°C)			±2	%	1
	CLK_SEL=1,2,3,4,5 and gyro active			±2	%	1

Table 4. A.C. Electrical Characteristics

Notes:

1. Derived from validation or characterization of parts, not guaranteed in production.
2. Guaranteed by design.
3. Production tested.

Other Electrical Specifications

Typical Operating Circuit of section 4.2, VDD = 1.8V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
SERIAL INTERFACE						
SPI Operating Frequency, All Registers Read/Write	Low Speed Characterization	100	100 ±10%		kHz	1,3
	High Speed Characterization	0.2	1	10	MHz	1, 2, 3
SPI Modes			0 and 3			
I^2C Operating Frequency	All registers, Fast-mode	100		400	kHz	1
	All registers, Standard-mode			100	kHz	1

Table 5. Other Electrical Specifications

Notes:

1. Derived from validation or characterization of parts, not guaranteed in production.
2. SPI clock duty cycle between 45% and 55% should be used for 10-MHz operation.
3. Minimum SPI/I^2C clock rate is dependent on ODR. If ODR is below 4 kHz, minimum clock rate is 100 kHz. If ODR is greater than 4 kHz, minimum clock rate is 200 kHz.

3.4 I²C TIMING CHARACTERIZATION

Typical Operating Circuit of section 4.2, VDD = 1.8V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

Parameters	Conditions	Min	Typical	Max	Units	Notes
I²C TIMING	**I²C FAST-MODE**					
f_{SCL}, SCL Clock Frequency		100		400	kHz	1
$t_{HD.STA}$, (Repeated) START Condition Hold Time		0.6			µs	1
t_{LOW}, SCL Low Period		1.3			µs	1
t_{HIGH}, SCL High Period		0.6			µs	1
$t_{SU.STA}$, Repeated START Condition Setup Time		0.6			µs	1
$t_{HD.DAT}$, SDA Data Hold Time		0			µs	1
$t_{SU.DAT}$, SDA Data Setup Time		100			ns	1
t_r, SDA and SCL Rise Time	C_b bus cap. from 10 to 400 pF	20+0.1C_b		300	ns	1
t_f, SDA and SCL Fall Time	C_b bus cap. from 10 to 400 pF	20+0.1C_b		300	ns	1
$t_{SU.STO}$, STOP Condition Setup Time		0.6			µs	1
t_{BUF}, Bus Free Time Between STOP and START Condition		1.3			µs	1
C_b, Capacitive Load for each Bus Line			< 400		pF	1
$t_{VD.DAT}$, Data Valid Time				0.9	µs	1
$t_{VD.ACK}$, Data Valid Acknowledge Time				0.9	µs	1

Table 6. I²C Timing Characteristics

Notes:

1. Based on characterization of 5 parts over temperature and voltage as mounted on evaluation board or in sockets

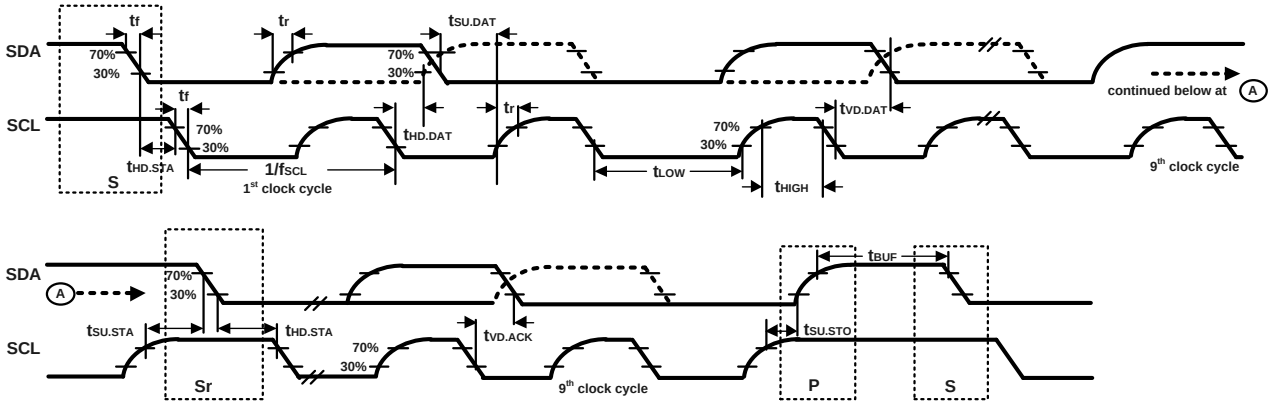


Figure 1. I²C Bus Timing Diagram

3.5 SPI TIMING CHARACTERIZATION

Typical Operating Circuit of section 4.2, VDD = 1.8V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

Parameter	Conditions	Min	Typ	Max	Units	Notes
SPI TIMING						
f_{SPC}, SPC Clock Frequency				10	MHz	1
t_{LOW}, SPC Low Period		45			ns	1
t_{HIGH}, SPC High Period		45			ns	1
$t_{SU.CS}$, CS Setup Time		2			ns	1
$t_{HD.CS}$, CS Hold Time		63			ns	1
$t_{SU.SDI}$, SDI Setup Time		3			ns	1
$t_{HD.SDI}$, SDI Hold Time		7			ns	1
$t_{VD.SDO}$, SDO Valid Time	C_{load} = 20pF			40	ns	1
$t_{DIS.SDO}$, SDO Output Disable Time				20	ns	1

Table 7. SPI Timing Characteristics (10 MHz Operation)

Notes:

1. Based on characterization of 5 parts over temperature and voltage as mounted on evaluation board or in sockets

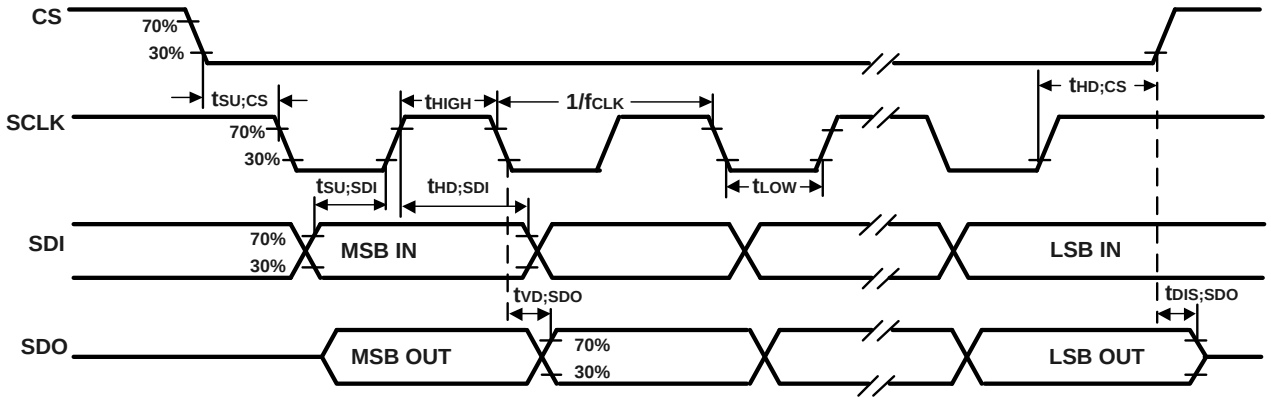


Figure 2. SPI Bus Timing Diagram

3.6 ABSOLUTE MAXIMUM RATINGS

Stress above those listed as “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to the absolute maximum ratings conditions for extended periods may affect device reliability.

Parameter	Rating
Supply Voltage, VDD	-0.5V to +4V
Supply Voltage, VDDIO	-0.5V to +4V
REGOUT	-0.5V to 2V
Input Voltage Level (SA0, FSYNC, SCL, SDA)	-0.5V to VDDIO + 0.5V
Acceleration (Any Axis, unpowered)	20,000g for 0.2 ms
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-40°C to +125°C
Electrostatic Discharge (ESD) Protection	2 kV (HBM); 250V (MM)
Latch-up	JEDEC Class II (2),125°C ±100 mA

Table 8. Absolute Maximum Ratings

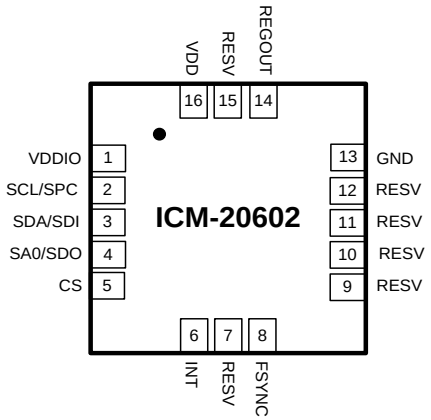
4 APPLICATIONS INFORMATION

4.1 PIN OUT DIAGRAM AND SIGNAL DESCRIPTION

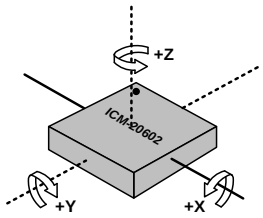
Pin Number	Pin Name	Pin Description
1	VDDIO	Digital I/O supply voltage
2	SCL/SPC	I²C serial clock (SCL); SPI serial clock (SPC)
3	SDA/SDI	I²C serial data (SDA); SPI serial data input (SDI)
4	SA0/SDO	I²C slave address LSB (SA0); SPI serial data output (SDO)
5	CS	Chip select (0 = SPI mode; 1 = I²C mode)
6	INT	Interrupt digital output (totem pole or open-drain)
7	RESV	Reserved. Do not connect.
8	FSYNC	Synchronization digital input (optional). Connect to GND if unused.
9	RESV	Reserved. Connect to GND.
10	RESV	Reserved. Connect to GND.
11	RESV	Reserved. Connect to GND.
12	RESV	Reserved. Connect to GND.
13	GND	Connect to GND
14	REGOUT	Regulator filter capacitor connection
15	RESV	Reserved. Connect to GND.
16	VDD	Power Supply

Table 9. Signal Descriptions

Note: Power up with SCL/SPC and CS pins held low is not a supported use case. In case this power up approach is used, software reset is required using the PWR_MGMT_1 register, prior to initialization.



LGA Package (Top View)
16-pin, 3mm x 3mm x 0.75mm
Typical Footprint and thickness



Orientation of Axes of Sensitivity and Polarity of Rotation

Figure 3. Pin out Diagram for ICM-20602 3 mm x 3 mm x 0.75 mm LGA

4.2 TYPICAL OPERATING CIRCUIT

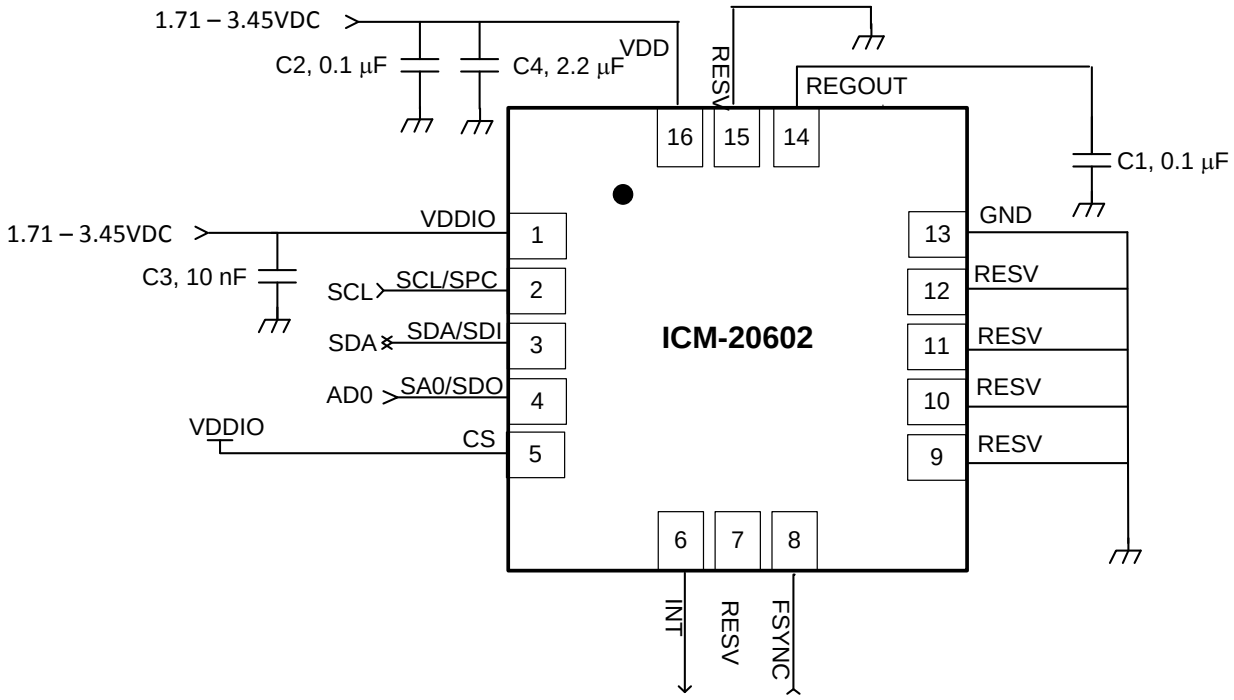


Figure 4. ICM-20602 Application Schematic

Note: I^2C lines are open drain and pullup resistors (e.g. 10 kΩ) are required.

4.3 BILL OF MATERIALS FOR EXTERNAL COMPONENTS

Component	Label	Specification	Quantity
REGOUT Capacitor	C1	X7R, 0.1 µF ±10%	1
VDD Bypass Capacitors	C2 C4	X7R, 0.1 µF ±10% X7R, 2.2 µF ±10%	1 1
VDDIO Bypass Capacitor	C3	X7R, 10 nF ±10%	1

Table 10. Bill of Materials

4.4 BLOCK DIAGRAM

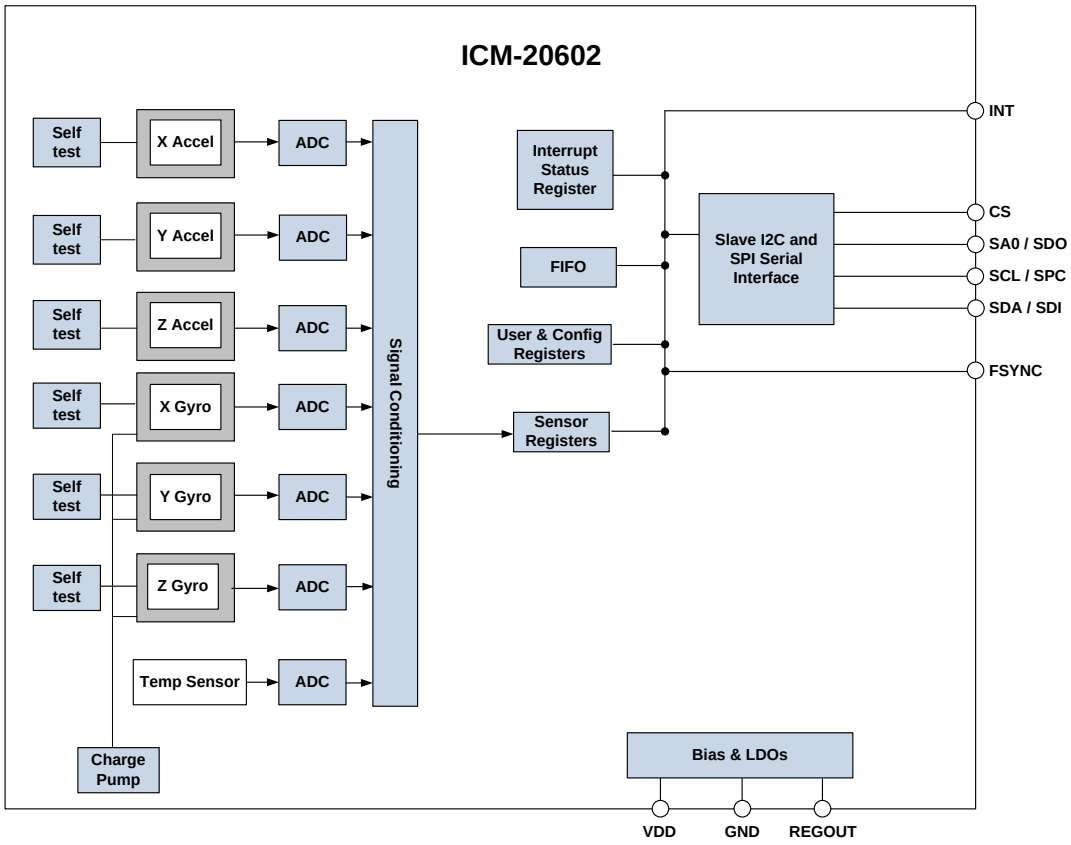


Figure 5. ICM-20602 Block Diagram

4.5 OVERVIEW

The ICM-20602 is comprised of the following key blocks and functions:

- Three-axis MEMS rate gyroscope sensor with 16-bit ADCs and signal conditioning
- Three-axis MEMS accelerometer sensor with 16-bit ADCs and signal conditioning
- I^2C and SPI serial communications interface
- Self-Test
- Clocking
- Sensor Data Registers
- FIFO
- Interrupts
- Digital-Output Temperature Sensor
- Bias and LDOs
- Charge Pump
- Standard Power Modes

4.6 THREE-AXIS MEMS GYROSCOPE WITH 16-BIT ADCS AND SIGNAL CONDITIONING

The ICM-20602 consists of three independent vibratory MEMS rate gyroscopes, which detect rotation about the X-, Y-, and Z- Axes. When the gyros are rotated about any of the sense axes, the Coriolis Effect causes a vibration that is detected by a capacitive pickoff. The resulting signal is amplified, demodulated, and filtered to produce a voltage that is proportional to the angular rate. This voltage is digitized using individual on-chip 16-bit Analog-to-Digital Converters (ADCs) to sample each axis. The full-scale range of the gyro sensors may be digitally programmed to ±250, ±500, ±1000, or ±2000 degrees per second (dps). The ADC sample rate is programmable from 8,000 samples per second, down to 3.9 samples per second, and user-selectable low-pass filters enable a wide range of cut-off frequencies.

4.7 THREE-AXIS MEMS ACCELEROMETER WITH 16-BIT ADCS AND SIGNAL CONDITIONING

The ICM-20602's 3-Axis accelerometer uses separate proof masses for each axis. Acceleration along a particular axis induces displacement on the corresponding proof mass, and capacitive sensors detect the displacement differentially. The ICM-20602's architecture reduces the accelerometers' susceptibility to fabrication variations as well as to thermal drift. When the device is placed on a flat surface, it will measure 0*g* on the X- and Y-axes and +1*g* on the Z-axis. The accelerometers' scale factor is calibrated at the factory and is nominally independent of supply voltage. Each sensor has a dedicated sigma-delta ADC for providing digital outputs. The full -scale range of the digital output can be adjusted to ±2*g*, ±4*g*, ±8*g*, or ±16*g*.

4.8 I²C AND SPI SERIAL COMMUNICATION INTERFACES

The ICM-20602 communicates to a system processor using either a SPI or an I²C serial interface. The ICM-20602 always acts as a slave when communicating to the system processor. The LSB of the I²C slave address is set by pin 4 (SA0).

ICM-20602 Solution Using I²C Interface

In Figure 6, the system processor is an I²C master to the ICM-20602.

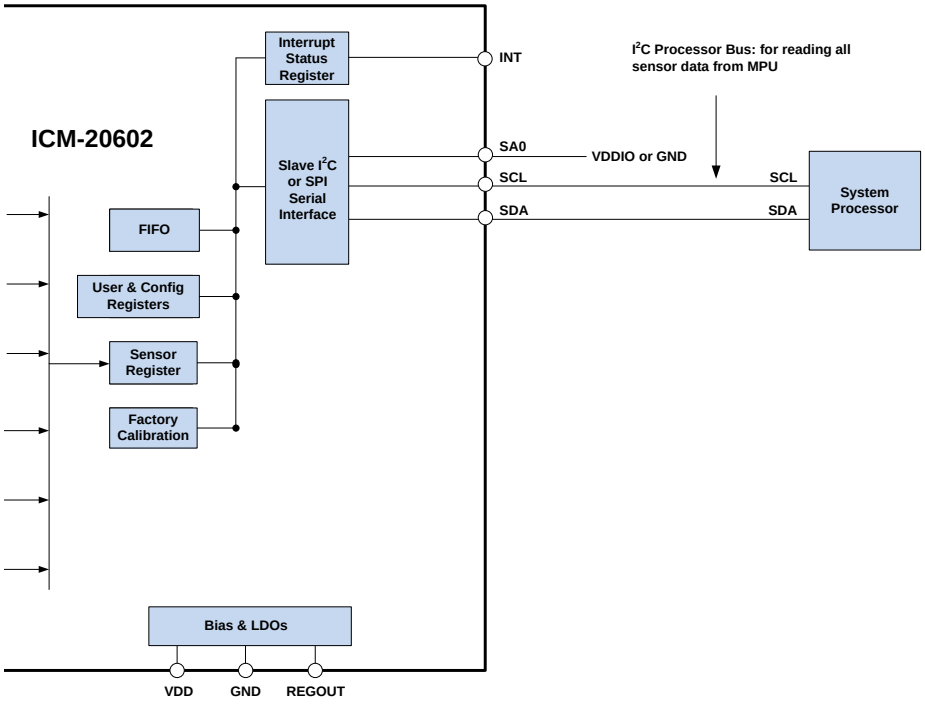


Figure 6. ICM-20602 Solution Using I²C Interface

ICM-20602 Solution Using SPI Interface

In the figure below, the system processor is an SPI master to the ICM-20602. Pins 2, 3, 4, and 5 are used to support the SPC, SDI, SDO, and CS signals for SPI communications.

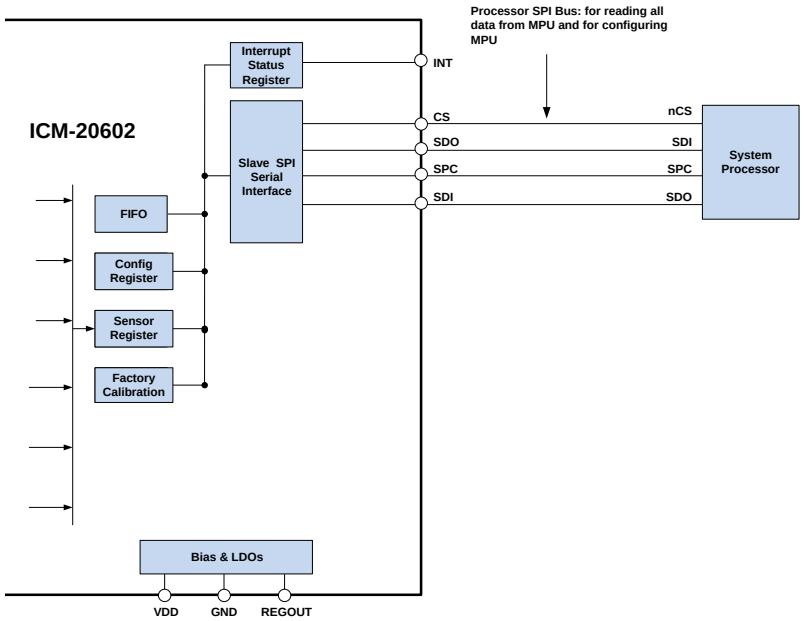


Figure 7. ICM-20602 Solution Using SPI Interface

4.9 SELF-TEST

Self-test allows for the testing of the mechanical and electrical portions of the sensors. The self-test for each measurement axis can be activated by means of the gyroscope and accelerometer self-test registers (registers 27 and 28).

When the self-test is activated, the electronics cause the sensors to be actuated and produce an output signal. The output signal is used to observe the self-test response.

The self-test response is defined as follows:

SELF-TEST RESPONSE = SENSOR OUTPUT WITH SELF-TEST ENABLED – SENSOR OUTPUT WITH SELF-TEST DISABLED

The self-test response for each gyroscope axis is defined in the gyroscope specification table, while that for each accelerometer axis is defined in the accelerometer specification table.

When the value of the self-test response is within the specified min/max limits of the product specification, the part has passed self-test. When the self-test response exceeds the min/max values, the part is deemed to have failed self-test.

For further information on Self-Test please refer to sections 8 and 9 of this document.

4.10 CLOCKING

The ICM-20602 has a flexible clocking scheme, allowing a variety of internal clock sources to be used for the internal synchronous circuitry. This synchronous circuitry includes the signal conditioning and ADCs, and various control circuits and registers. An on-chip PLL provides flexibility in the allowable inputs for generating this clock.

Allowable internal sources for generating the internal clock are:

a) An internal relaxation oscillator

b) Auto-select between internal relaxation oscillator and gyroscope MEMS oscillator to use the best available source

The only setting supporting specified performance in all modes is option b). It is recommended that option b) be used.

4.11 SENSOR DATA REGISTERS

The sensor data registers contain the latest gyroscope, accelerometer, and temperature measurement data. They are read-only registers, and are accessed via the serial interface. Data from these registers may be read anytime.

4.12 FIFO

The ICM-20602 contains a 1 KB FIFO (FIFO depth 1008 bytes) register that is accessible via the Serial Interface. The FIFO configuration register determines which data is written into the FIFO. Possible choices include gyro data, accelerometer data, temperature readings, and FSYNC input. A FIFO counter keeps track of how many bytes of valid data are contained in the FIFO. The FIFO register supports burst reads. The interrupt function may be used to determine when new data is available.
The ICM-20602 allows FIFO read in low-power accelerometer mode. A programmable FIFO watermark is included, with data-ready interrupt triggered when the watermark is reached.

4.13 INTERRUPTS

Interrupt functionality is configured via the Interrupt Configuration register. Items that are configurable include the INT and DRDY pins configuration, the interrupt latching and clearing method, and triggers for the interrupt. Items that can trigger an interrupt are (1) Clock generator locked to new reference oscillator (used when switching clock sources); (2) new data is available to be read (from the FIFO and Data registers); (3) accelerometer event interrupts; (4) FIFO watermark; (5) FIFO overflow. The interrupt status can be read from the Interrupt Status register.
For further information regarding interrupts, please refer to sections 8 and 9 of this document.

4.14 DIGITAL-OUTPUT TEMPERATURE SENSOR

An on-chip temperature sensor and ADC are used to measure the ICM-20602 die temperature. The readings from the ADC can be read from the FIFO or the Sensor Data registers.

4.15 BIAS AND LDOS

The bias and LDO section generates the internal supply and the reference voltages and currents required by the ICM-20602. Its two inputs are an unregulated VDD and a VDDIO logic reference supply voltage. The LDO output is bypassed by a capacitor at REGOUT. For further details on the capacitor, please refer to the Bill of Materials for External Components.

4.16 CHARGE PUMP

An on-chip charge pump generates the high voltage required for the MEMS oscillator.

4.17 STANDARD POWER MODES – UPDATE THE POWER MODES

The following table lists the user-accessible power modes for ICM-20602.

Mode	Name	Gyro	Accel
1	Sleep Mode	Off	Off
2	Standby Mode	Drive On	Off
3	Accelerometer Low-Power Mode	Off	Duty-Cycled
4	Accelerometer Low-Noise Mode	Off	On
5	Gyroscope Low-Power Mode	Duty-Cycled	Off
6	Gyroscope Low-Noise Mode	On	Off
7	6-Axis Low-Noise Mode	On	On
8	6-Axis Low-Power Mode	Duty-Cycled	On

Table 11. Standard Power Modes for ICM-20602

Notes: Power consumption for individual modes can be found in section 0

5 PROGRAMMABLE INTERRUPTS

The ICM-20602 has a programmable interrupt system which can generate an interrupt signal on the INT and DRDY pins. Status flags indicate the source of an interrupt. Interrupt sources may be enabled and disabled individually.

Interrupt Name	Module
Motion Detection	Motion
FIFO Overflow	FIFO
FIFO Watermark	FIFO
Data Ready	Sensor Registers

Table 12. Table of Interrupt Sources

For information regarding the interrupt enable/disable registers and flag registers, please refer to sections 11 and 12 of this document. Some interrupt sources are explained below.

5.1 WAKE-ON-MOTION INTERRUPT

The ICM-20602 provides motion detection capability. A qualifying motion sample is one where the high passed sample from any axis has an absolute value exceeding a user-programmable threshold. The following steps explain how to configure the Wake-on-Motion Interrupt.

Step 1: Ensure that Accelerometer is running

- In PWR_MGMT_1 register (0x6B) set CYCLE = 0, SLEEP = 0, and GYRO_STANDBY = 0
- In PWR_MGMT_2 register (0x6C) set STBY_XA = STBY_YA = STBY_ZA = 0, and STBY_XG = STBY_YG = STBY_ZG = 1

Step 2: Accelerometer Configuration

- In ACCEL_CONFIG2 register (0x1D) set ACCEL_FCHOICE_B = 1 and A_DLPF_CFG[2:0] = 1 (b001)

Step 3: Enable Motion Interrupt

- In INT_ENABLE register (0x38) set WOM_X_INT_EN = WOM_Y_INT_EN = WOM_Z_INT_EN = 1 to enable motion interrupt for X, Y, and Z axis

Step 4: Set Motion Threshold

- Set the motion threshold for X-axis in ACCEL_WOM_X_THR register (0x20)
- Set the motion threshold for Y-axis in ACCEL_WOM_Y_THR register (0x21)
- Set the motion threshold for Z-axis in ACCEL_WOM_Z_THR register (0x22)

Step 5: Set Interrupt Mode

- In ACCEL_INTEL_CTRL register (0x69) clear bit 0 (WOM_TH_MODE) to select the motion interrupt as an OR of the enabled interrupts for X, Y, Z-axes and set bit 0 to make the interrupt an AND of the enabled interrupts for X, Y, Z axes

Step 6: Enable Accelerometer Hardware Intelligence

- In ACCEL_INTEL_CTRL register (0x69) set ACCEL_INTEL_EN = ACCEL_INTEL_MODE = 1

Step 7: Set Frequency of Wake-Up

- In SMPLRT_DIV register (0x19) set SMPLRT_DIV[7:0] = 3.9Hz – 500Hz

Step 8: Enable Cycle Mode (Accelerometer Low-Power Mode)

- In PWR_MGMT_1 register (0x6B) set CYCLE = 1

6 DIGITAL INTERFACE

6.1 I²C AND SPI SERIAL INTERFACES

The internal registers and memory of the ICM-20602 can be accessed using either I²C at 400 kHz or SPI at 10MHz. SPI operates in four-wire mode.

Pin Number	Pin Name	Pin Description
2	SCL / SPC	I²C serial clock (SCL); SPI serial clock (SPC)
3	SDA / SDI	I²C serial data (SDA); SPI serial data input (SDI)
4	SA0 / SDO	I²C Slave Address LSB (SA0); SPI serial data output (SDO)
5	CS	Chip select (0 = SPI mode)

Table 13. Serial Interface

Note: To prevent switching into I2C mode when using SPI, the I2C interface should be disabled by setting the *I2C_IF_DIS* configuration bit at I2C_IF. Setting this bit should be performed immediately after waiting for the time specified by the "Start-Up Time for Register Read/Write" in Section 3.3.2. For further information regarding the *I2C_IF_DIS* bit at I2C_IF register, please refer to sections 10 and 11 of this document.

6.2 I²C INTERFACE

I²C is a two-wire interface comprised of the signals serial data (SDA) and serial clock (SCL). In general, the lines are open-drain and bi-directional. In a generalized I²C interface implementation, attached devices can be a master or a slave. The master device puts the slave address on the bus, and the slave device with the matching address acknowledges the master.

The ICM-20602 always operates as a slave device when communicating to the system processor, which thus acts as the master. SDA and SCL lines typically need pull-up resistors to VDD. The maximum bus speed is 400 kHz.

The slave address of the ICM-20602 is b110100X which is 7 bits long. The LSB bit of the 7 bit address is determined by the logic level on pin SA0. This allows two ICM-20602s to be connected to the same I²C bus. When used in this configuration, the address of one of the devices should be b1101000 (pin SA0 is logic low) and the address of the other should be b1101001 (pin SA0 is logic high).

6.3 I²C COMMUNICATIONS PROTOCOL

START (S) and STOP (P) Conditions

Communication on the I²C bus starts when the master puts the START condition (S) on the bus, which is defined as a HIGH-to-LOW transition of the SDA line while SCL line is HIGH (see figure below). The bus is considered to be busy until the master puts a STOP condition (P) on the bus, which is defined as a LOW to HIGH transition on the SDA line while SCL is HIGH (see figure below). Additionally, the bus remains busy if a repeated START (Sr) is generated instead of a STOP condition.

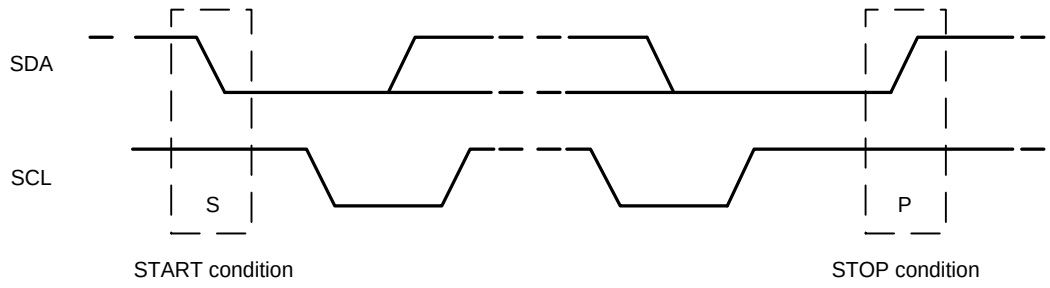


Figure 8. START and STOP Conditions

Data Format / Acknowledge

I²C data bytes are defined to be 8-bits long. There is no restriction to the number of bytes transmitted per data transfer. Each byte transferred must be followed by an acknowledge (ACK) signal. The clock for the acknowledge signal is generated by the master, while the receiver generates the actual acknowledge signal by pulling down SDA and holding it low during the HIGH portion of the acknowledge clock pulse.

If a slave is busy and cannot transmit or receive another byte of data until some other task has been performed, it can hold SCL LOW, thus forcing the master into a wait state. Normal data transfer resumes when the slave is ready, and releases the clock line (refer to the following figure).

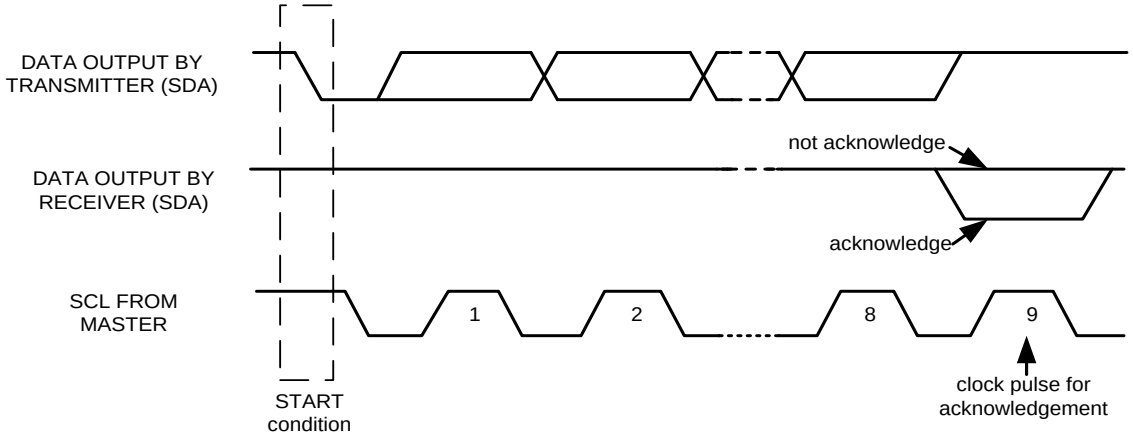


Figure 9. Acknowledge on the I²C Bus

Communications

After beginning communications with the START condition (S), the master sends a 7-bit slave address followed by an 8th bit, the read/write bit. The read/write bit indicates whether the master is receiving data from or is writing to the slave device. Then, the master releases the SDA line and waits for the acknowledge signal (ACK) from the slave device. Each byte transferred must be followed by an acknowledge bit. To acknowledge, the slave device pulls the SDA line LOW and keeps it LOW for the high period of the SCL line. Data transmission is always terminated by the master with a STOP condition (P), thus freeing the communications line. However, the master can generate a repeated START condition (Sr), and address another slave without first generating a STOP condition (P). A LOW to HIGH transition on the SDA line while SCL is HIGH defines the stop condition. All SDA changes should take place when SCL is low, with the exception of start and stop conditions.

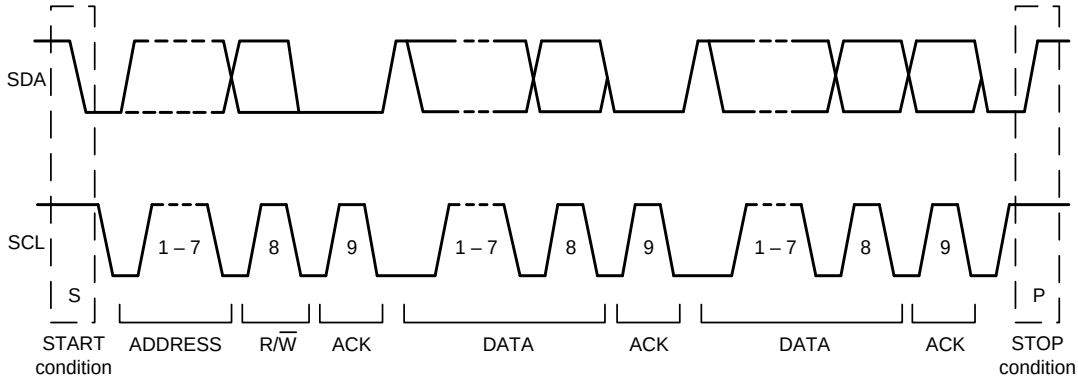


Figure 10. Complete I²C Data Transfer

To write the internal ICM-20602 registers, the master transmits the start condition (S), followed by the I²C address and the write bit (0). At the 9th clock cycle (when the clock is high), the ICM-20602 acknowledges the transfer. Then the master puts the register address (RA) on the bus. After the ICM-20602 acknowledges the reception of the register address, the master puts the register data onto the bus. This is followed by the ACK signal, and data transfer may be concluded by the stop condition (P). To write multiple bytes after the last ACK signal, the master can continue outputting data rather than transmitting a stop signal. In this case, the ICM-20602 automatically increments the register address and loads the data to the appropriate register. The following figures show single and two-byte write sequences.

Single-Byte Write Sequence

Master	S	AD+W		RA		DATA		P
Slave			ACK		ACK		ACK	

Burst Write Sequence

Master	S	AD+W		RA		DATA		DATA		P
Slave			ACK		ACK		ACK		ACK	

To read the internal ICM-20602 registers, the master sends a start condition, followed by the I^2C address and a write bit, and then the register address that is going to be read. Upon receiving the ACK signal from the ICM-20602, the master transmits a start signal followed by the slave address and read bit. As a result, the ICM-20602 sends an ACK signal and the data. The communication ends with a not acknowledge (NACK) signal and a stop bit from master. The NACK condition is defined such that the SDA line remains high at the 9th clock cycle. The following figures show single and two-byte read sequences.

Single-Byte Read Sequence

Master	S	AD+W		RA		S	AD+R			NACK	P
Slave			ACK		ACK			ACK	DATA		

Burst Read Sequence

Master	S	AD+W		RA		S	AD+R			ACK		NACK	P
Slave			ACK		ACK			ACK	DATA		DATA		

6.4 I^2C TERMS

Signal	Description
S	Start Condition: SDA goes from high to low while SCL is high
AD	Slave I^2C address
W	Write bit (0)
R	Read bit (1)
ACK	Acknowledge: SDA line is low while the SCL line is high at the 9th clock cycle
NACK	Not-Acknowledge: SDA line stays high at the 9th clock cycle
RA	ICM-20602 internal register address
DATA	Transmit or received data
P	Stop condition: SDA going from low to high while SCL is high

Table 14. I^2C Terms

6.5 SPI INTERFACE

SPI is a 4-wire synchronous serial interface that uses two control lines and two data lines. The ICM-20602 always operates as a Slave device during standard Master-Slave SPI operation.

With respect to the Master, the Serial Clock output (SPC), the Serial Data Output (SDO) and the Serial Data Input (SDI) are shared among the Slave devices. Each SPI slave device requires its own Chip Select (CS) line from the master.

CS goes low (active) at the start of transmission and goes back high (inactive) at the end. Only one CS line is active at a time, ensuring that only one slave is selected at any given time. The CS lines of the non-selected slave devices are held high, causing their SDO lines to remain in a high-impedance (high-z) state so that they do not interfere with any active devices.

SPI Operational Features

1. Data is delivered MSB first and LSB last
2. Data is latched on the rising edge of SPC
3. Data should be transitioned on the falling edge of SPC
4. The maximum frequency of SPC is 10MHz
5. SPI read and write operations are completed in 16 or more clock cycles (two or more bytes). The first byte contains the SPI Address, and the following byte(s) contain(s) the SPI data. The first bit of the first byte contains the Read/Write bit and indicates the Read (1) or Write (0) operation. The following 7 bits contain the Register Address. In cases of multiple-byte Read/Writes, data is two or more bytes:

SPI Address format

MSB							**LSB**
R/W	A6	A5	A4	A3	A2	A1	A0

SPI Data format

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0

6. Supports Single or Burst Read/Writes.

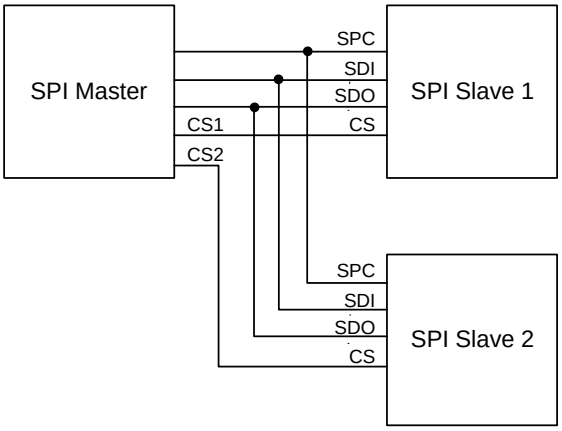


Figure 11. Typical SPI Master/Slave Configuration

7 SERIAL INTERFACE CONSIDERATIONS

7.1 ICM-20602 SUPPORTED INTERFACES

The ICM-20602 supports I^2C communications on its serial interface. The ICM-20602's I/O logic levels are set to be VDDIO.

The figure below depicts a sample circuit of ICM-20602. It shows the relevant logic levels and voltage connections.

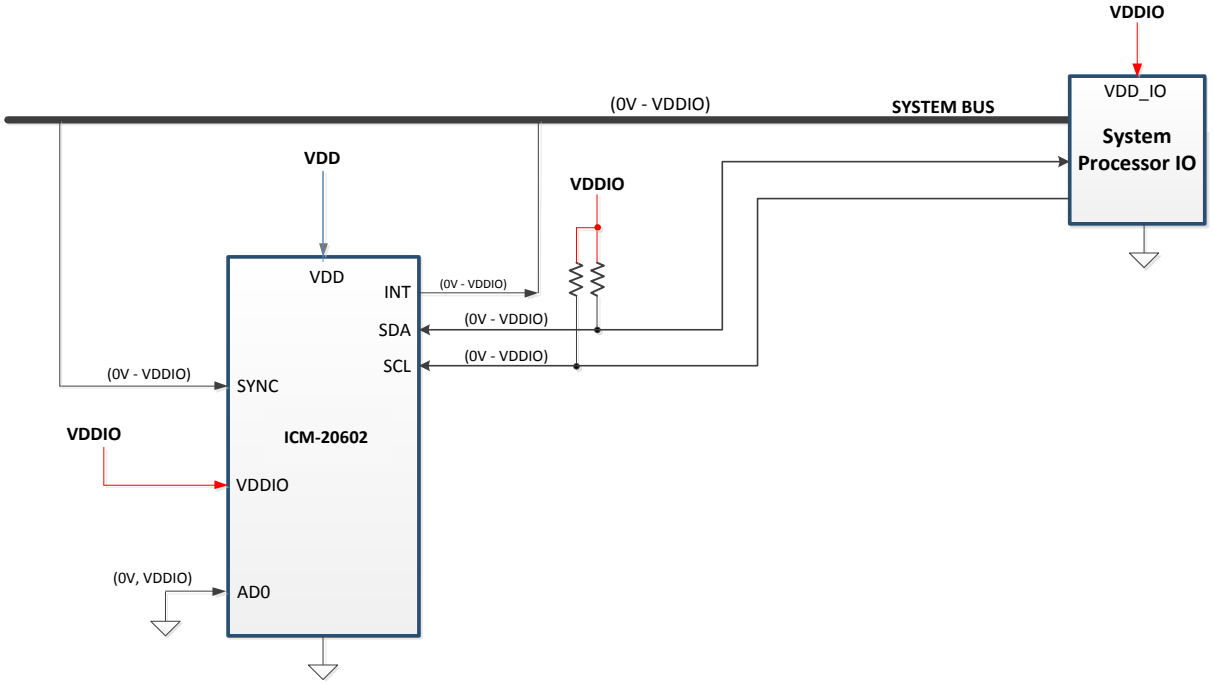


Figure 12. I/O Levels and Connections

8 REGISTER MAP

The following table lists the register map for the ICM-20602. Note that all registers are accessible in all modes of device operation.

Addr (Hex)	Addr (Dec.)	Register Name	Serial I/F	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
04	04	XG_OFFS_TC_H	READ/ WRITE	XG_OFFS_LP[5:0]						XG_OFFS_TC_H [9:8]	
05	05	XG_OFFS_TC_L	READ/ WRITE	XG_OFFS_TC_L [7:0]							
07	07	YG_OFFS_TC_H	READ/ WRITE	YG_OFFS_LP[5:0]						YG_OFFS_TC_H [9:8]	
08	08	YG_OFFS_TC_L	READ/ WRITE	YG_OFFS_TC_L [7:0]							
0A	10	ZG_OFFS_TC_H	READ/ WRITE	ZG_OFFS_LP[5:0]						ZG_OFFS_TC_H [9:8]	
0B	11	ZG_OFFS_TC_L	READ/ WRITE	ZG_OFFS_TC_L [7:0]							
0D	13	SELF_TEST_X_ACCEL	READ/ WRITE	XA_ST_DATA[7:0]							
0E	14	SELF_TEST_Y_ACCEL	READ/ WRITE	YA_ST_DATA[7:0]							
0F	15	SELF_TEST_Z_ACCEL	READ/ WRITE	ZA_ST_DATA[7:0]							
13	19	XG_OFFS_USRH	READ/ WRITE	X_OFFS_USR [15:8]							
14	20	XG_OFFS_USRL	READ/ WRITE	X_OFFS_USR [7:0]							
15	21	YG_OFFS_USRH	READ/ WRITE	Y_OFFS_USR [15:8]							
16	22	YG_OFFS_USRL	READ/ WRITE	Y_OFFS_USR [7:0]							
17	23	ZG_OFFS_USRH	READ/ WRITE	Z_OFFS_USR [15:8]							
18	24	ZG_OFFS_USRL	READ/ WRITE	Z_OFFS_USR [7:0]							
19	25	SMPLRT_DIV	READ/ WRITE	SMPLRT_DIV[7:0]							
1A	26	CONFIG	READ/ WRITE	-	FIFO_ MODE	EXT_SYNC_SET[2:0]			DLPF_CFG[2:0]		
1B	27	GYRO_CONFIG	READ/ WRITE	XG_ST	YG_ST	ZG_ST	FS_SEL [1:0]		-	FCHOICE_B[1:0]	
1C	28	ACCEL_CONFIG	READ/ WRITE	XA_ST	YA_ST	ZA_ST	ACCEL_FS_SEL[1:0]		-		
1D	29	ACCEL_CONFIG 2	READ/ WRITE	-		DEC2_CFG		ACCEL_FCH OICE_B	A_DLPF_CFG		
1E	30	LP_MODE_CFG	READ/ WRITE	GYRO_CYC LE	G_AVGCFG[2:0]			-			
20	32	ACCEL_WOM_X_THR	READ/ WRITE	WOM_X_TH[7:0]							
21	33	ACCEL_WOM_Y_THR	READ/ WRITE	WOM_Y_TH[7:0]							
22	34	ACCEL_WOM_Z_THR	READ/ WRITE	WOM_Z_TH[7:0]							
23	35	FIFO_EN	READ/ WRITE	-			GYRO_FIFO_EN	ACCEL_FIF O_EN	-		
36	54	FSYNC_INT	READ to CLEAR	FSYNC_INT	-						
37	55	INT_PIN_CFG	READ/ WRITE	INT_LEVEL	INT_OPEN	LATCH _INT_EN	INT_RD _CLEAR	FSYNC_INT _LEVEL	FSYNC _INT_MODE _EN	-	
38	56	INT_ENABLE	READ/ WRITE	WOM_X_I NT_EN	WOM_Y_INT _EN	WOM_Z_INT _EN	FIFO _OFLOW _EN	-	GDRIVE_INT _EN	-	DATA_RDY_IN T_EN
39	57	FIFO_WM_INT_STATUS	READ to CLEAR	-	FIFO_WM_IN T	-					

Addr (Hex)	Addr (Dec.)	Register Name	Serial I/F	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
3A	58	INT_STATUS	READ to CLEAR	WOM_X_INT	WOM_Y_INT	WOM_Z_INT	FIFO_OFLOW_INT	-	GDRIVE_INT	-	DATA_RDY_INT
3B	59	ACCEL_XOUT_H	READ	ACCEL_XOUT[15:8]							
3C	60	ACCEL_XOUT_L	READ	ACCEL_XOUT[7:0]							
3D	61	ACCEL_YOUT_H	READ	ACCEL_YOUT[15:8]							
3E	62	ACCEL_YOUT_L	READ	ACCEL_YOUT[7:0]							
3F	63	ACCEL_ZOUT_H	READ	ACCEL_ZOUT[15:8]							
40	64	ACCEL_ZOUT_L	READ	ACCEL_ZOUT[7:0]							
41	65	TEMP_OUT_H	READ	TEMP_OUT[15:8]							
42	66	TEMP_OUT_L	READ	TEMP_OUT[7:0]							
43	67	GYRO_XOUT_H	READ	GYRO_XOUT[15:8]							
44	68	GYRO_XOUT_L	READ	GYRO_XOUT[7:0]							
45	69	GYRO_YOUT_H	READ	GYRO_YOUT[15:8]							
46	70	GYRO_YOUT_L	READ	GYRO_YOUT[7:0]							
47	71	GYRO_ZOUT_H	READ	GYRO_ZOUT[15:8]							
48	72	GYRO_ZOUT_L	READ	GYRO_ZOUT[7:0]							
50	80	SELF_TEST_X_GYRO	READ/ WRITE	XG_ST_DATA[7:0]							
51	81	SELF_TEST_Y_GYRO	READ/ WRITE	YG_ST_DATA[7:0]							
52	82	SELF_TEST_Z_GYRO	READ/ WRITE	ZG_ST_DATA[7:0]							
60	96	FIFO_WM_TH1	READ/ WRITE	-						FIFO_WM_TH[9:8]	
61	97	FIFO_WM_TH2	READ/ WRITE	FIFO_WM_TH[7:0]							
68	104	SIGNAL_PATH_RESET	READ/ WRITE	-						ACCEL_RST	TEMP_RST
69	105	ACCEL_INTEL_CTRL	READ/ WRITE	ACCEL_INTEL_EN	ACCEL_INTEL_MODE	-				OUTPUT_LIMIT	WOM_TH_MODE
6A	106	USER_CTRL	READ/ WRITE	-	FIFO_EN	-			FIFO_RST	-	SIG_COND_RST
6B	107	PWR_MGMT_1	READ/ WRITE	DEVICE_RESET	SLEEP	CYCLE	GYRO_STANDBY	TEMP_DIS	CLKSEL[2:0]		
6C	108	PWR_MGMT_2	READ/ WRITE	-		STBY_XA	STBY_YA	STBY_ZA	STBY_XG	STBY_YG	STBY_ZG
70	112	I2C_IF	READ/ WRITE	-	I2C_IF_DIS	-					
72	114	FIFO_COUNTH	READ	FIFO_COUNT[15:8]							
73	115	FIFO_COUNTL	READ	FIFO_COUNT[7:0]							
74	116	FIFO_R_W	READ/ WRITE	FIFO_DATA[7:0]							
75	117	WHO_AM_I	READ	WHOAMI[7:0]							
77	119	XA_OFFSET_H	READ/ WRITE	XA_OFFS [14:7]							
78	120	XA_OFFSET_L	READ/ WRITE	XA_OFFS [6:0]							-
7A	122	YA_OFFSET_H	READ/ WRITE	YA_OFFS [14:7]							
7B	123	YA_OFFSET_L	READ/ WRITE	YA_OFFS [6:0]							-
7D	125	ZA_OFFSET_H	READ/ WRITE	ZA_OFFS [14:7]							
7E	126	ZA_OFFSET_L	READ/ WRITE	ZA_OFFS [6:0]							-

Table 15. Register Map

Note: Register Names ending in _H and _L contain the high and low bytes, respectively, of an internal register value.

The reset value is 0x00 for all registers other than the registers below, also the self-test registers contain pre-programmed values and will not be 0x00 after reset.

- Register 26 (0x80) CONFIG
- Register 107 (0x41) Power Management 1
- Register 117 (0x12) WHO_AM_I

9 REGISTER DESCRIPTIONS

This section describes the function and contents of each register within the ICM-20602.
Note: The device will come up in sleep mode upon power-up.

9.1 REGISTER DESCRIPTIONS

Reset values are "0" for all registers, unless otherwise specified

9.2 REGISTER 04 – GYROSCOPE LOW NOISE TO LOW POWER OFFSET SHIFT AND GYROSCOPE OFFSET TEMPERATURE COMPENSATION (TC) REGISTER

Register Name: XG_OFFS_TC_H

Register Type: READ/WRITE

Register Address: 04 (Decimal); 04 (Hex)

BIT	NAME	FUNCTION
[7:2]	XG_OFFS_LP[5:0]	Stores the offset shift in the gyroscope output from low noise mode to low power mode to be implemented as a correction in the customer software. 2's complement digital code, 0.125 dps/LSB from +3.875dps to -4dps.
[1:0]	XG_OFFS_TC_H[9:8]	Bits 9 and 8 of the 10-bit offset of X gyroscope (2's complement)

9.3 REGISTER 05 – GYROSCOPE LOW NOISE TO LOW POWER OFFSET SHIFT AND GYROSCOPE OFFSET TEMPERATURE COMPENSATION (TC) REGISTER

Register Name: XG_OFFS_TC_L

Type: READ/WRITE

Register Address: 05 (Decimal); 05 (Hex)

BIT	NAME	FUNCTION
[7:0]	XG_OFFS_TC_L[7:0]]	Bits 7 to 0 of the 10-bit offset of X gyroscope (2's complement)

Description:

The temperature compensation (TC) registers are used to reduce gyro offset variation due to temperature change. The TC feature is always enabled. However, the compensation only happens when a TC coefficient is programed during factory trim which gets loaded into these registers at power up or after a *DEVICE_RESET*. If these registers contain a value of zero, temperature compensation has no effect on the offset of the chip. The TC registers have a 10-bit magnitude and sign adjustment in all full-scale modes with a resolution of 2.52 mdps/C steps.

If these registers contain a non-zero value after power up, the user may write zeros to them to see the offset values without TC with temperature variation. Note that doing so may result in offset values that exceed data sheet "Initial ZRO Tolerance" in other than normal ambient temperature (~25°C). The TC coefficients maybe restored by the user with a power up or a *DEVICE_RESET*.

The above description also applies to registers 7-8 and 10-11.

9.4 REGISTER 07 – GYROSCOPE LOW NOISE TO LOW POWER OFFSET SHIFT AND GYROSCOPE OFFSET TEMPERATURE COMPENSATION (TC) REGISTER

Register Name: YG_OFFS_TC_H

Register Type: READ/WRITE

Register Address: 07 (Decimal); 07 (Hex)

BIT	NAME	FUNCTION
[7:2]	YG_OFFS_LP[5:0]	Stores the offset shift in the gyroscope output from low noise mode to low power mode to be implemented as a correction in the customer software. 2's complement digital code, 0.125dps/LSB from +3.875dps to -4dps.
[1:0]	YG_OFFS_TC_H[9:8]	Bits 9 and 8 of the 10-bit offset of Y gyroscope (2's complement)

9.5 REGISTER 08 – GYROSCOPE LOW NOISE TO LOW POWER OFFSET SHIFT AND GYROSCOPE OFFSET TEMPERATURE COMPENSATION (TC) REGISTER

Register Name: YG_OFFS_TC_L
Register Type: READ/WRITE
Register Address: 08 (Decimal); 08 (Hex)

BIT	NAME	FUNCTION
[7:0]	YG_OFFS_TC_L[7:0]]	Bits 7 to 0 of the 10-bit offset of Y gyroscope (2's complement)

9.6 REGISTER 10 – GYROSCOPE LOW NOISE TO LOW POWER OFFSET SHIFT AND GYROSCOPE OFFSET TEMPERATURE COMPENSATION (TC) REGISTER

Register Name: ZG_OFFS_TC_H
Register Type: READ/WRITE
Register Address: 10 (Decimal); 0A (Hex)

BIT	NAME	FUNCTION
[7:2]	ZG_OFFS_LP[5:0]	Stores the offset shift in the gyroscope output from low noise mode to low power mode to be implemented as a correction in the customer software. 2's complement digital code, 0.125dps/LSB from +3.875dps to -4dps.
[1:0]	ZG_OFFS_TC_H[9:8]	Bits 9 and 8 of the 10-bit offset of Z gyroscope (2's complement)

9.7 REGISTER 11 – GYROSCOPE LOW NOISE TO LOW POWER OFFSET SHIFT AND GYROSCOPE OFFSET TEMPERATURE COMPENSATION (TC) REGISTER

Register Name: ZG_OFFS_TC_L
Register Type: READ/WRITE
Register Address: 11 (Decimal); 0B (Hex)

BIT	NAME	FUNCTION
[7:0]	ZG_OFFS_TC_L[7:0]]	Bits 7 to 0 of the 10-bit offset of Z gyroscope (2's complement)

9.8 REGISTERS 13 TO 15 ACCELEROMETER SELF-TEST REGISTERS

Register Name: SELF_TEST_X_ACCEL, SELF_TEST_Y_ACCEL, SELF_TEST_Z_ACCEL
Type: READ/WRITE
Register Address: 13, 14, 15 (Decimal); 0D, 0E, 0F (Hex)

REGISTER	BIT	NAME	FUNCTION
SELF_TEST_X_ACCEL	**[7:0]**	XA_ST_DATA[7:0]	The value in this register indicates the self-test output generated during manufacturing tests. This value is to be used to check against subsequent self-test outputs performed by the end user.
SELF_TEST_Y_ACCEL	**[7:0]**	YA_ST_DATA[7:0]	The value in this register indicates the self-test output generated during manufacturing tests. This value is to be used to check against subsequent self-test outputs performed by the end user.
SELF_TEST_Z_ACCEL	**[7:0]**	ZA_ST_DATA[7:0]	The value in this register indicates the self-test output generated during manufacturing tests. This value is to be used to check against subsequent self-test outputs performed by the end user.

The equation to convert self-test codes in OTP to factory self-test measurement is:

$$ST\_OTP = (2620/2^{FS}) * 1.01^{(ST\_code-1)} \text{ (lsb)}$$

where ST_OTP is the value that is stored in OTP of the device, FS is the Full Scale value, and ST_code is based on the Self-Test value (ST_ FAC) determined in TDK-InvenSense's factory final test and calculated based on the following equation:

$$ST\_code = round\left(\frac{\log(ST\_FAC/(2620/2^{FS}))}{\log(1.01)}\right) + 1$$

9.9 REGISTER 19 – X-GYRO OFFSET ADJUSTMENT REGISTER: HIGH BYTE

Register Name: XG_OFFS_USRH
Register Type: READ/WRITE
Register Address: 19 (Decimal); 13 (Hex)

BIT	NAME	FUNCTION
[7:0]	X_OFFS_USR[15:8]	Bits 15 to 8 of the 16-bit offset of X gyroscope (2's complement). This register is used to remove DC bias from the sensor output. The value in this register is added to the gyroscope sensor value before going into the sensor register.

9.10 REGISTER 20 – X-GYRO OFFSET ADJUSTMENT REGISTER: LOW BYTE

Register Name: XG_OFFS_USRL
Register Type: READ/WRITE
Register Address: 20 (Decimal); 14 (Hex)

BIT	NAME	FUNCTION
[7:0]	X_OFFS_USR[7:0]	Bits 7 to 0 of the 16-bit offset of X gyroscope (2's complement). This register is used to remove DC bias from the sensor output. The value in this register is added to the gyroscope sensor value before going into the sensor register.

9.11 REGISTER 21 – Y-GYRO OFFSET ADJUSTMENT REGISTER: HIGH BYTE

Register Name: YG_OFFS_USRH
Register Type: READ/WRITE
Register Address: 21 (Decimal); 15 (Hex)

BIT	NAME	FUNCTION
[7:0]	Y_OFFS_USR[15:8]	Bits 15 to 8 of the 16-bit offset of Y gyroscope (2's complement). This register is used to remove DC bias from the sensor output. The value in this register is added to the gyroscope sensor value before going into the sensor register.

9.12 REGISTER 22 – Y-GYRO OFFSET ADJUSTMENT REGISTER: LOW BYTE

Register Name: YG_OFFS_USRL
Register Type: READ/WRITE
Register Address: 22 (Decimal); 16 (Hex)

BIT	NAME	FUNCTION
[7:0]	Y_OFFS_USR[7:0]	Bits 7 to 0 of the 16-bit offset of Y gyroscope (2's complement). This register is used to remove DC bias from the sensor output. The value in this register is added to the gyroscope sensor value before going into the sensor register.

9.13 REGISTER 23 – Z-GYRO OFFSET ADJUSTMENT REGISTER: HIGH BYTE

Register Name: ZG_OFFS_USRH
Register Type: READ/WRITE
Register Address: 23 (Decimal); 17 (Hex)

BIT	NAME	FUNCTION
[7:0]	Z_OFFS_USR[15:8]	Bits 15 to 8 of the 16-bit offset of Z gyroscope (2's complement). This register is used to remove DC bias from the sensor output. The value in this register is added to the gyroscope sensor value before going into the sensor register.

9.14 REGISTER 24 – Z-GYRO OFFSET ADJUSTMENT REGISTER: LOW BYTE

Register Name: ZG_OFFS_USRL
Register Type: READ/WRITE
Register Address: 24 (Decimal); 18 (Hex)

BIT	NAME	FUNCTION
[7:0]	Z_OFFS_USR[7:0]	Bits 7 to 0 of the 16-bit offset of Z gyroscope (2's complement). This register is used to remove DC bias from the sensor output. The value in this register is added to the gyroscope sensor value before going into the sensor register.

9.15 REGISTER 25 – SAMPLE RATE DIVIDER

Register Name: SMPLRT_DIV
Register Type: READ/WRITE
Register Address: 25 (Decimal); 19 (Hex)

BIT	NAME	FUNCTION
[7:0]	SMPLRT_DIV[7:0]	Divides the internal sample rate (see register CONFIG) to generate the sample rate that controls sensor data output rate, FIFO sample rate. **NOTE**: This register is only effective when FCHOICE_B register bits are 2'b00, and (0 < DLPF_CFG < 7). This is the update rate of the sensor register: SAMPLE_RATE = INTERNAL_SAMPLE_RATE / (1 + SMPLRT_DIV) Where INTERNAL_SAMPLE_RATE = 1 kHz

9.16 REGISTER 26 – CONFIGURATION

Register Name: CONFIG
Register Type: READ/WRITE
Register Address: 26 (Decimal); 1A (Hex)

BIT	NAME	FUNCTION
[7]	-	Default configuration value is 1. User should set it to 0.
[6]	FIFO_MODE	When set to '1', when the FIFO is full, additional writes will not be written to FIFO. When set to '0', when the FIFO is full, additional writes will be written to the FIFO, replacing the oldest data.
[5:3]	EXT_SYNC_SET[2:0]	Enables the FSYNC pin data to be sampled. **EXT_SYNC_SET** / **FSYNC bit location** 0 – function disabled 1 – TEMP_OUT_L[0] 2 – GYRO_XOUT_L[0] 3 – GYRO_YOUT_L[0] 4 – GYRO_ZOUT_L[0] 5 – ACCEL_XOUT_L[0] 6 – ACCEL_YOUT_L[0] 7 – ACCEL_ZOUT_L[0] FSYNC will be latched to capture short strobes. This will be done such that if FSYNC toggles, the latched value toggles, but won't toggle again until the new latched value is captured by the sample rate strobe.
[2:0]	DLPF_CFG[2:0]	For the DLPF to be used, FCHOICE_B[1:0] is 2'b00. See the table below.

The DLPF is configured by *DLPF_CFG,* when *FCHOICE_B* [1:0] = 2b'00. The gyroscope and temperature sensor are filtered according to the value of *DLPF_CFG* and *FCHOICE_B* as shown in the table below.

FCHOICE_B		DLPF_CFG	Gyroscope			Temperature Sensor
<1>	<0>		3-dB BW (Hz)	Noise BW (Hz)	Rate (kHz)	3-dB BW (Hz)
X	1	X	8173	8595.1	32	4000
1	0	X	3281	3451.0	32	4000
0	0	0	250	306.6	8	4000
0	0	1	176	177.0	1	188
0	0	2	92	108.6	1	98
0	0	3	41	59.0	1	42
0	0	4	20	30.5	1	20
0	0	5	10	15.6	1	10
0	0	6	5	8.0	1	5
0	0	7	3281	3451.0	8	4000

9.17 REGISTER 27 – GYROSCOPE CONFIGURATION

Register Name: GYRO_CONFIG

Register Type: READ/WRITE

Register Address: 27 (Decimal); 1B (Hex)

BIT	NAME	FUNCTION
[7]	XG_ST	X Gyro self-test
[6]	YG_ST	Y Gyro self-test
[5]	ZG_ST	Z Gyro self-test
[4:3]	FS_SEL[1:0]	Gyro Full Scale Select: 00 = ±250 dps 01= ±500 dps 10 = ±1000 dps 11 = ±2000 dps
[2]	-	Reserved
[1:0]	FCHOICE_B[1:0]	Used to bypass DLPF as shown in table 1 above.

9.18 REGISTER 28 – ACCELEROMETER CONFIGURATION

Register Name: ACCEL_CONFIG

Register Type: READ/WRITE

Register Address: 28 (Decimal); 1C (Hex)

BIT	NAME	FUNCTION
[7]	XA_ST	X Accel self-test
[6]	YA_ST	Y Accel self-test
[5]	ZA_ST	Z Accel self-test
[4:3]	ACCEL_FS_SEL[1:0]	Accel Full Scale Select: ±2g (00), ±4g (01), ±8g (10), ±16g (11)
[2:0]	-	Reserved

9.19 REGISTER 29 – ACCELEROMETER CONFIGURATION 2

Register Name: ACCEL_CONFIG2

Register Type: READ/WRITE

Register Address: 29 (Decimal); 1D (Hex)

BIT	NAME	FUNCTION
[5:4]	DEC2_CFG[1:0]	Averaging filter settings for Low Power Accelerometer mode: 0 = Average 4 samples 1 = Average 8 samples 2 = Average 16 samples 3 = Average 32 samples
[3]	ACCEL_FCHOICE_B	Used to bypass DLPF as shown in the table below.
[2:0]	A_DLPF_CFG	Accelerometer low pass filter setting as shown in table 2 below.

Accelerometer Data Rates and Bandwidths (Low-Noise Mode)

ACCEL_FCHOICE_B	A_DLPF_CFG	Accelerometer		
		3-dB BW (Hz)	Noise BW (Hz)	Rate (kHz)
1	X	1046.0	1100.0	4
0	0	218.1	235.0	1
0	1	218.1	235.0	1
0	2	99.0	121.3	1
0	3	44.8	61.5	1
0	4	21.2	31.0	1
0	5	10.2	15.5	1
0	6	5.1	7.8	1
0	7	420.0	441.6	1

The data output rate of the DLPF filter block can be further reduced by a factor of 1/(1+SMPLRT_DIV), where SMPLRT_DIV is an 8-bit integer. Following is a small subset of ODRs that are configurable for the accelerometer in the low-noise mode in this manner (Hz):

3.91, 7.81, 15.63, 31.25, 62.50, 125, 250, 500, 1K

The following table lists the approximate accelerometer filter bandwidths available in the low-power mode of operation for some example ODRs.

In the low-power mode of operation, the accelerometer is duty-cycled. The following table shows some example configurations for accelerometer low power mode.

	Averages	1x	4x	8x	16x	32x
	ACCEL_FCHOICE_B	1	0	0	0	0
	DEC2_CFG	X	0	1	2	3
	A_DLPF_CFG	X	7	7	7	7
	Ton (ms)	1.084	1.84	2.84	4.84	8.84
	NBW (Hz)	1100	442	236	122	62
	3-dB BW (Hz)	1046	420	219	111	56
	Noise TYP (mg-rms)	3.3	2.1	1.5	1.1	0.79
SMPLRT_DIV	ODR (Hz)	Low-Power Accelerometer Mode Current Consumption (µA)				
255	3.91	9.4	10.2	11.5	13.8	18.5
127	7.81	10.7	12.4	14.7	19.6	28.9
99	10	11.4	13.7	16.6	22.6	34.7
63	15.63	13.3	16.7	21.5	30.8	49.7
31	31.25	18.3	25.4	34.8	53.6	91.2
19	50	24.4	35.8	50.8	80.8	141.1
15	62.5	28.4	42.7	61.5	99.0	174.3
9	100	40.7	63.5	93.6	153.7	303.3
7	125	48.8	77.4	114.8	190.1	N/A
4	200	73.4	118.8	178.9	299.3	
3	250	89.6	146.5	221.6	N/A	
1	500	171.1	284.9	N/A		

9.20 REGISTER 30 – GYROSCOPE LOW POWER MODE CONFIGURATION

Register Name: LP_MODE_CFG

Register Type: READ/WRITE

Register Address: 30 (Decimal); 1E (Hex)

BIT	NAME	FUNCTION
[7]	GYRO_CYCLE	When set to '1' low-power gyroscope mode is enabled. Default setting is '0'
[6:4]	G_AVGCFG[2:0]	Averaging filter configuration for low-power gyroscope mode. Default setting is '000'
[3:0]	-	Reserved

To operate in gyroscope low-power mode or 6-axis low-power mode, GYRO_CYCLE should be set to '1.' Gyroscope filter configuration is determined by G_AVGCFG[2:0] that sets the averaging filter configuration. It is not dependent on DLPF_CFG[2:0].

The following table shows some example configurations for gyroscope low power mode.

	Averages	1x	2x	4x	8x	16x	32x	64x	128x
	G_AVGCFG	0	1	2	3	4	5	6	7
	NBW (Hz)	650.8	407.1	224.2	117.4	60.2	30.6	15.6	8.0
	3-dB BW (Hz)	622	391	211	108	54	27	14	7
	Noise TYP (dps-rms)	0.10	0.08	0.06	0.04	0.03	0.02	0.016	0.011
SMPLRT_DIV	ODR (Hz)	Low-Power Gyroscope Mode Current Consumption (mA)							
255	3.9	0.79	0.80	0.80	0.82	0.85	0.90	1.01	1.23
99	10.0	0.81	0.82	0.84	0.87	0.95	1.09	1.37	1.94
65	15.2	0.83	0.84	0.87	0.92	1.03	1.24	1.67	2.53
64	15.4	0.83	0.84	0.87	0.92	1.03	1.25	1.69	N/A
33	29.4	0.87	0.90	0.95	1.05	1.26	1.68	2.51	N/A
32	30.3	0.87	0.90	0.95	1.06	1.28	1.70	N/A	N/A
19	50.0	0.93	0.98	1.06	1.24	1.60	2.30	N/A	N/A
17	55.6	0.95	1.00	1.10	1.29	1.69	2.47	N/A	N/A
16	58.8	0.96	1.01	1.11	1.32	1.74	N/A	N/A	N/A
9	100.0	1.08	1.17	1.35	1.70	2.41	N/A	N/A	N/A
7	125.0	1.16	1.27	1.49	1.93	N/A	N/A	N/A	N/A
6	142.9	1.21	1.34	1.59	2.09	N/A	N/A	N/A	N/A
4	200.0	1.38	1.56	1.91	N/A	N/A	N/A	N/A	N/A
3	250.0	1.53	1.75	2.19	N/A	N/A	N/A	N/A	N/A
2	333.3	1.78	2.07	N/A	N/A	N/A	N/A	N/A	N/A

9.21 REGISTER 32 – WAKE-ON MOTION THRESHOLD: X-AXIS ACCELEROMETER

Register Name: ACCEL_WOM_X_THR
Register Type: READ/WRITE
Register Address: 32 (Decimal); 20 (Hex)

BIT	NAME	FUNCTION
[7:0]	WOM_X_TH[7:0]	This register holds the threshold value for the Wake on Motion Interrupt for X-axis accelerometer.

9.22 REGISTER 33 – WAKE-ON MOTION THRESHOLD: Y-AXIS ACCELEROMETER

Register Name: ACCEL_WOM_Y_THR
Register Type: READ/WRITE
Register Address: 33 (Decimal); 21 (Hex)

BIT	NAME	FUNCTION
[7:0]	WOM_Y_TH[7:0]	This register holds the threshold value for the Wake on Motion Interrupt for Y-axis accelerometer.

9.23 REGISTER 34 – WAKE-ON MOTION THRESHOLD: Z-AXIS ACCELEROMETER

Register Name: ACCEL_WOM_Z_THR
Register Type: READ/WRITE
Register Address: 34 (Decimal); 22 (Hex)

BIT	NAME	FUNCTION
[7:0]	WOM_Z_TH[7:0]	This register holds the threshold value for the Wake on Motion Interrupt for Z-axis accelerometer.

9.24 REGISTER 35 – FIFO ENABLE

Register Name: FIFO_EN
Register Type: READ/WRITE
Register Address: 35 (Decimal); 23 (Hex)

BIT	NAME	FUNCTION
[7:5]	-	Reserved
[4]	GYRO_FIFO_EN	1 – write TEMP_OUT_H, TEMP_OUT_L, GYRO_XOUT_H, GYRO_XOUT_L, GYRO_YOUT_H, GYRO_YOUT_L, GYRO_ZOUT_H, and GYRO_ZOUT_L to the FIFO at the sample rate; If enabled, buffering of data occurs even if data path is in standby. 0 – function is disabled
[3]	ACCEL_FIFO_EN	1 – write ACCEL_XOUT_H, ACCEL_XOUT_L, ACCEL_YOUT_H, ACCEL_YOUT_L, ACCEL_ZOUT_H, ACCEL_ZOUT_L, TEMP_OUT_H, and TEMP_OUT_L to the FIFO at the sample rate; 0 – function is disabled
[2:0]	-	Reserved

NOTE: If both GYRO_FIFO_EN And ACCEL_FIFO_EN are 1, write ACCEL_XOUT_H, ACCEL_XOUT_L, ACCEL_YOUT_H, ACCEL_YOUT_L, ACCEL_ZOUT_H, ACCEL_ZOUT_L, TEMP_OUT_H, TEMP_OUT_L, GYRO_XOUT_H, GYRO_XOUT_L, GYRO_YOUT_H, GYRO_YOUT_L, GYRO_ZOUT_H, and GYRO_ZOUT_L to the FIFO at the sample rate.

9.25 REGISTER 54 – FSYNC INTERRUPT STATUS

Register Name: FSYNC_INT
Register Type: READ to CLEAR
Register Address: 54 (Decimal); 36 (Hex)

BIT	NAME	FUNCTION
[7]	FSYNC_INT	This bit automatically sets to 1 when a FSYNC interrupt has been generated. The bit clears to 0 after the register has been read.

9.26 REGISTER 55 – INT/DRDY PIN / BYPASS ENABLE CONFIGURATION

Register Name: INT_PIN_CFG
Register Type: READ/WRITE
Register Address: 55 (Decimal); 37 (Hex)

BIT	NAME	FUNCTION
[7]	INT_LEVEL	1 – The logic level for INT/DRDY pin is active low. 0 – The logic level for INT/DRDY pin is active high.
[6]	INT_OPEN	1 – INT/DRDY pin is configured as open drain. 0 – INT/DRDY pin is configured as push-pull.
[5]	LATCH_INT_EN	1 – INT/DRDY pin level held until interrupt status is cleared. 0 – INT/DRDY pin indicates interrupt pulse's width is 50us.
[4]	INT_RD_CLEAR	1 – Interrupt status is cleared if any read operation is performed. 0 – Interrupt status is cleared only by reading INT_STATUS register
[3]	FSYNC_INT_LEVEL	1 – The logic level for the FSYNC pin as an interrupt is active low. 0 – The logic level for the FSYNC pin as an interrupt is active high.
[2]	FSYNC_INT_MODE_EN	When this bit is equal to 1, the FSYNC pin will trigger an interrupt when it transitions to the level specified by F*SYNC_INT_LEVEL*. When this bit is equal to 0, the FSYNC pin is disabled from causing an interrupt.
[1:0]	-	Reserved.

9.27 REGISTER 56 – INTERRUPT ENABLE

Register Name: INT_ENABLE
Register Type: READ/WRITE
Register Address: 56 (Decimal); 38 (Hex)

BIT	NAME	FUNCTION
[7]	WOM_X_INT_EN	1 – Enable WoM interrupt on X-axis accelerometer. Default setting is 0.
[6]	WOM_Y_INT_EN	1 – Enable WoM interrupt on Y-axis accelerometer. Default setting is 0.
[5]	WOM_Z_INT_EN	1 – Enable WoM interrupt on Z-axis accelerometer. Default setting is 0.
[4]	FIFO_OFLOW_EN	1 – Enables a FIFO buffer overflow to generate an interrupt. 0 – Function is disabled.
[3]	-	Reserved
[2]	GDRIVE_INT_EN	Gyroscope Drive System Ready interrupt enable
[1]	-	Reserved
[0]	DATA_RDY_INT_EN	Data ready interrupt enable

9.28 REGISTER 57 – FIFO WATERMARK INTERRUPT STATUS

Register Name: FIFO_WM_INT_STATUS
Register Type: READ to CLEAR
Register Address: 57 (Decimal); 39 (Hex)

BIT	NAME	FUNCTION
[6]	FIFO_WM_INT	FIFO Watermark interrupt status. Cleared on Read.

9.29 REGISTER 58 – INTERRUPT STATUS

Register Name: INT_STATUS
Register Type: READ to CLEAR
Register Address: 58 (Decimal); 3A (Hex)

BIT	NAME	FUNCTION
[7]	WOM_X_INT	X-axis accelerometer WoM interrupt status. Cleared on Read.
[6]	WOM_Y_INT	Y-axis accelerometer WoM interrupt status. Cleared on Read.
[5]	WOM_Z_INT	Z-axis accelerometer WoM interrupt status. Cleared on Read.
[4]	FIFO_OFLOW_INT	This bit automatically sets to 1 when a FIFO buffer overflow has been generated. The bit clears to 0 after the register has been read.
[3]	-	Reserved.
[2]	GDRIVE_INT	Gyroscope Drive System Ready interrupt
[1]	-	Reserved
[0]	DATA_RDY_INT	This bit automatically sets to 1 when a Data Ready interrupt is generated. The bit clears to 0 after the register has been read.

9.30 REGISTERS 59 TO 64 – ACCELEROMETER MEASUREMENTS: X-AXIS HIGH BYTE

Register Name: ACCEL_XOUT_H
Register Type: READ only
Register Address: 59 (Decimal); 3B (Hex)

BIT	NAME	FUNCTION
[7:0]	ACCEL_XOUT[15:8]	High byte of accelerometer x-axis data.

Register Name: ACCEL_XOUT_L
Register Type: READ only
Register Address: 60 (Decimal); 3C (Hex)

BIT	NAME	FUNCTION
[7:0]	ACCEL_XOUT[7:0]	Low byte of accelerometer x-axis data.

Register Name: ACCEL_YOUT_H

Register Type: READ only

Register Address: 61 (Decimal); 3D (Hex)

BIT	NAME	FUNCTION
[7:0]	ACCEL_YOUT[15:8]	High byte of accelerometer y-axis data.

Register Name: ACCEL_YOUT_L

Register Type: READ only

Register Address: 62 (Decimal); 3E (Hex)

BIT	NAME	FUNCTION
[7:0]	ACCEL_YOUT[7:0]	Low byte of accelerometer y-axis data.

Register Name: ACCEL_ZOUT_H

Register Type: READ only

Register Address: 63 (Decimal); 3F (Hex)

BIT	NAME	FUNCTION
[7:0]	ACCEL_ZOUT[15:8]	High byte of accelerometer z-axis data.

Register Name: ACCEL_ZOUT_L

Register Type: READ only

Register Address: 64 (Decimal); 40 (Hex)

BIT	NAME	FUNCTION
[7:0]	ACCEL_ZOUT[7:0]	Low byte of accelerometer z-axis data.

9.31 REGISTERS 65 TO 66 – TEMPERATURE MEASUREMENT

Register Name: TEMP_OUT_H

Register Type: READ only

Register Address: 65 (Decimal); 41 (Hex)

BIT	NAME	FUNCTION
[7:0]	TEMP_OUT[15:8]	Low byte of the temperature sensor output

Register Name: TEMP_OUT_L

Register Type: READ only

Register Address: 66 (Decimal); 42 (Hex)

BIT	NAME	FUNCTION
[7:0]	TEMP_OUT[7:0]	High byte of the temperature sensor output **TEMP_degC** = (TEMP_OUT[15:0]/Temp_Sensitivity) + RoomTemp_Offset where Temp_Sensitivity = 326.8 LSB/ºC and RoomTemp_Offset = 25ºC

9.32 REGISTERS 67 TO 72 – GYROSCOPE MEASUREMENT

Register Name: GYRO_XOUT_H

Register Type: READ only

Register Address: 67 (Decimal); 43 (Hex)

BIT	NAME	FUNCTION
[7:0]	GYRO_XOUT[15:8]	High byte of the X-Axis gyroscope output

Register Name: GYRO_XOUT_L

Register Type: READ only

Register Address: 68 (Decimal); 44 (Hex)

BIT	NAME	FUNCTION
[7:0]	GYRO_XOUT[7:0]	Low byte of the X-Axis gyroscope output **GYRO_XOUT =** Gyro_Sensitivity * X_angular_rate Nominal Conditions: FS_SEL = 0 Gyro_Sensitivity = 131 LSB/(º/s)

Register Name: GYRO_YOUT_H

Register Type: READ only

Register Address: 69 (Decimal); 45 (Hex)

BIT	NAME	FUNCTION
[7:0]	GYRO_YOUT[15:8]	High byte of the Y-Axis gyroscope output

Register Name: GYRO_YOUT_L

Register Type: READ only

Register Address: 70 (Decimal); 46 (Hex)

BIT	NAME	FUNCTION
[7:0]	GYRO_YOUT[7:0]	Low byte of the Y-Axis gyroscope output **GYRO_YOUT =** Gyro_Sensitivity * Y_angular_rate Nominal Conditions FS_SEL = 0 Gyro_Sensitivity = 131 LSB/(º/s)

Register Name: GYRO_ZOUT_H

Register Type: READ only

Register Address: 71 (Decimal); 47 (Hex)

BIT	NAME	FUNCTION
[7:0]	GYRO_ZOUT[15:8]	High byte of the Z-Axis gyroscope output

Register Name: GYRO_ZOUT_L

Register Type: READ only

Register Address: 72 (Decimal); 48 (Hex)

BIT	NAME	FUNCTION
[7:0]	GYRO_ZOUT[7:0]	Low byte of the Z-Axis gyroscope output **GYRO_ZOUT =** Gyro_Sensitivity * Z_angular_rate Nominal Conditions FS_SEL = 0 Gyro_Sensitivity = 131 LSB/(º/s)

9.33 REGISTER 80 TO 82 – GYROSCOPE SELF-TEST REGISTERS

Register Name: SELF_TEST_X_GYRO, SELF_TEST_Y_GYRO, SELF_TEST_Z_GYRO

Type: READ/WRITE

Register Address: 80, 81, 82 (Decimal); 50, 51, 52 (Hex)

REGISTER	BIT	NAME	FUNCTION
SELF_TEST_X_GYRO	[7:0]	XG_ST_DATA[7:0]	The value in this register indicates the self-test output generated during manufacturing tests. This value is to be used to check against subsequent self-test outputs performed by the end user.
SELF_TEST_Y_GYRO	[7:0]	YG_ST_DATA[7:0]	The value in this register indicates the self-test output generated during manufacturing tests. This value is to be used to check against subsequent self-test outputs performed by the end user.
SELF_TEST_Z_GYRO	[7:0]	ZG_ST_DATA[7:0]	The value in this register indicates the self-test output generated during manufacturing tests. This value is to be used to check against subsequent self-test outputs performed by the end user.

The equation to convert self-test codes in OTP to factory self-test measurement is:

$$ST\_OTP = (2620/2^{FS}) * 1.01^{(ST\_code-1)} \text{ (lsb)}$$

where ST_OTP is the value that is stored in OTP of the device, FS is the Full Scale value, and ST_code is based on the Self-Test value (ST_ FAC) determined in TDK-InvenSense's factory final test and calculated based on the following equation:

$$ST\_code = round\left(\frac{\log(ST\_FAC/(2620/2^{FS}))}{\log(1.01)}\right) + 1$$

9.34 REGISTER 96 TO 97 – FIFO WATERMARK THRESHOLD IN NUMBER OF BYTES

Register Name: FIFO_WM_TH1

Register Type: READ/WRITE

Register Address: 96 (Decimal); 60 (Hex)

BIT	NAME	FUNCTION
[1:0]	FIFO_WM_TH[9:8]	FIFO watermark threshold in number of bytes. Watermark interrupt is disabled if the threshold is set to "0". Default value is 00000000.

Register Name: FIFO_WM_TH2

Register Type: READ/WRITE

Register Address: 97 (Decimal); 61 (Hex)

BIT	NAME	FUNCTION
[7:0]	FIFO_WM_TH[7:0]	FIFO watermark threshold in number of bytes. Watermark interrupt is disabled if the threshold is set to "0". Default value is 00000000.

The register FIFO_WM_TH[9:0] sets the FIFO watermark threshold level (0 - 1023). User should ensure that bit 7 of register 0x1A is set to 0 before using this feature. When the FIFO count is at or above the watermark level (FIFO_COUNT[15:0] ≥ FIFO_WM_TH[9:0]) and the system is not in the middle of a FIFO read, an interrupt is triggered. The interrupt will set the FIFO watermark interrupt status register field FIFO_WM_INT = 1, and the INT pin will issue a pulse if configured in pulse mode, or set to the active level if configured in latch mode. Register bit FIFO_WM_INT is not read-to-clear, unlike the other interrupts. Rather, whenever FIFO_R_W register is read, FIFO_WM_INT status bit is cleared automatically. At the same time, the INT pin will be cleared as well if it is configured in latch mode.

The FIFO watermark interrupt and the INT pin are cleared upon the first read (and only the first read) of the FIFO. If, at the end of the FIFO read, the FIFO count is at or above the watermark level, the interrupt status bit and INT pin will again be set. If the INT pin is configured for latched operation, it will wait until the host completes the read to set to the active level.

9.35 REGISTER 104 – SIGNAL PATH RESET

Register Name: SIGNAL_PATH_RESET

Register Type: READ/WRITE

Register Address: 104 (Decimal); 68 (Hex)

BIT	NAME	FUNCTION
[7:2]	-	Reserved
[1]	ACCEL_RST	Reset accel digital signal path. **NOTE**: Sensor registers are not cleared. Use SIG_COND_RST to clear sensor registers.
[0]	TEMP_RST	Reset temp digital signal path. **NOTE**: Sensor registers are not cleared. Use SIG_COND_RST to clear sensor registers.

9.36 REGISTER 105 – ACCELEROMETER INTELLIGENCE CONTROL

Register Name: ACCEL_INTEL_CTRL

Register Type: READ/WRITE

Register Address: 105 (Decimal); 69 (Hex)

BIT	NAME	FUNCTION
[7]	ACCEL_INTEL_EN	This bit enables the Wake-on-Motion detection logic
[6]	ACCEL_INTEL_MODE	0 – Do not use 1 – Compare the current sample with the previous sample
[5:2]	-	Reserved
[1]	OUTPUT_LIMIT	To avoid limiting sensor output to less than 0x7FFF, set this bit to 1. This should be done every time the ICM-20602 is powered up.
[0]	WOM_TH_MODE	0 – Set WoM interrupt on the OR of all enabled accelerometer thresholds 1 – Set WoM interrupt on the AND of all enabled accelerometer threshold Default setting is 0

9.37 REGISTER 106 – USER CONTROL

Register Name: USER_CTRL
Register Type: READ/WRITE
Register Address: 106 (Decimal); 6A (Hex)

BIT	NAME	FUNCTION
[7]	-	Reserved
[6]	FIFO_EN	1 – Enable FIFO operation mode. 0 – Disable FIFO access from serial interface.
[5]	-	Reserved
[4]	-	Reserved
[3]	-	Reserved
[2]	FIFO_RST	1 – Reset FIFO module. Reset is asynchronous. This bit auto clears after one clock cycle of the internal 20 MHz clock.
[1]	-	Reserved
[0]	SIG_COND_RST	1 – Reset all gyro digital signal path, accel digital signal path, and temp digital signal path. This bit also clears all the sensor registers.

9.38 REGISTER 107 – POWER MANAGEMENT 1

Register Name: PWR_MGMT_1
Register Type: READ/WRITE
Register Address: 107 (Decimal); 6B (Hex)

BIT	NAME	FUNCTION
[7]	DEVICE_RESET	1 – Reset the internal registers and restores the default settings. The bit automatically clears to 0 once the reset is done.
[6]	SLEEP	When set to 1, the chip is set to sleep mode.
[5]	CYCLE	When set to 1, and SLEEP and STANDBY are not set to 1, the chip will cycle between sleep and taking a single accelerometer sample at a rate determined by SMPLRT_DIV **NOTE**: When all accelerometer axes are disabled via PWR_MGMT_2 register bits and cycle is enabled, the chip will wake up at the rate determined by the respective registers above, but will not take any samples.
[4]	GYRO_STANDBY	When set, the gyro drive and pll circuitry are enabled, but the sense paths are disabled. This is a low power mode that allows quick enabling of the gyros.
[3]	TEMP_DIS	When set to 1, this bit disables the temperature sensor.
[2:0]	CLKSEL[2:0]	

Code	Clock Source
0	Internal 20 MHz oscillator
1	Auto selects the best available clock source – PLL if ready, else use the Internal oscillator
2	Auto selects the best available clock source – PLL if ready, else use the Internal oscillator
3	Auto selects the best available clock source – PLL if ready, else use the Internal oscillator
4	Auto selects the best available clock source – PLL if ready, else use the Internal oscillator
5	Auto selects the best available clock source – PLL if ready, else use the Internal oscillator
6	Internal 20 MHz oscillator
7	Stops the clock and keeps timing generator in reset

NOTE: The default value of CLKSEL[2:0] is 001. It is required that CLKSEL[2:0] be set to 001 to achieve full gyroscope performance.

9.39 REGISTER 108 – POWER MANAGEMENT 2

Register Name: PWR_MGMT_2

Register Type: READ/WRITE

Register Address: 108 (Decimal); 6C (Hex)

BIT	NAME	FUNCTION
[7]	-	Reserved
[6]	-	Reserved
[5]	STBY_XA	1 – X accelerometer is disabled 0 – X accelerometer is on
[4]	STBY_YA	1 – Y accelerometer is disabled 0 – Y accelerometer is on
[3]	STBY_ZA	1 – Z accelerometer is disabled 0 – Z accelerometer is on
[2]	STBY_XG	1 – X gyro is disabled 0 – X gyro is on
[1]	STBY_YG	1 – Y gyro is disabled 0 – Y gyro is on
[0]	STBY_ZG	1 – Z gyro is disabled 0 – Z gyro is on

9.40 REGISTER 112 – I^2C INTERFACE

Register Name: I2C_IF

Register Type: READ/WRITE

Register Address: 112 (Decimal); 70 (Hex)

BIT	NAME	FUNCTION
[7]	-	Reserved
[6]	I2C_IF_DIS	1 – Disable I2C Slave module and put the serial interface in SPI mode only.
[5:0]	-	Reserved

9.41 REGISTER 114 AND 115 – FIFO COUNT REGISTERS

Register Name: FIFO_COUNTH

Register Type: READ Only

Register Address: 114 (Decimal); 72 (Hex)

BIT	NAME	FUNCTION
[7:0]	FIFO_COUNT[15:8]	High Bits, count indicates the number of written bytes in the FIFO. Reading this byte latches the data for both FIFO_COUNTH, and FIFO_COUNTL.

Register Name: FIFO_COUNTL

Register Type: READ Only

Register Address: 115 (Decimal); 73 (Hex)

BIT	NAME	FUNCTION
[7:0]	FIFO_COUNT[7:0]	Low Bits, count indicates the number of written bytes in the FIFO. **NOTE**: Must read FIFO_COUNTL to latch new data for both FIFO_COUNTH and FIFO_COUNTL.

9.42 REGISTER 116 – FIFO READ WRITE

Register Name: FIFO_R_W

Register Type: READ/WRITE

Register Address: 116 (Decimal); 74 (Hex)

BIT	NAME	FUNCTION
[7:0]	FIFO_DATA[7:0]	Read/Write command provides Read or Write operation for the FIFO.

Description:

This register is used to read and write data from the FIFO buffer.

Data is written to the FIFO in order of register number (from lowest to highest). If all the FIFO enable flags (see below) are enabled, the contents of registers 59 through 72 will be written in order at the Sample Rate.

The contents of the sensor data registers (Registers 59 to 72) are written into the FIFO buffer when their corresponding FIFO enable flags are set to 1 in FIFO_EN (Register 35).

If the FIFO buffer has overflowed, the status bit *FIFO_OFLOW_INT* is automatically set to 1. This bit is located in INT_STATUS (Register 58). When the FIFO buffer has overflowed, the oldest data will be lost and new data will be written to the FIFO unless register 26 CONFIG, bit[6] FIFO_MODE = 1.

If the FIFO buffer is empty, reading register FIFO_DATA will return a unique value of 0xFF until new data is available. Normal data is precluded from ever indicating 0xFF, so 0xFF gives a trustworthy indication of FIFO empty.

9.43 REGISTER 117 – WHO AM I

Register Name: WHO_AM_I

Register Type: READ only

Register Address: 117 (Decimal); 75 (Hex)

BIT	NAME	FUNCTION
[7:0]	WHOAMI	Register to indicate to user which device is being accessed.

This register is used to verify the identity of the device. The contents of *WHOAMI* is an 8-bit device ID. The default value of the register is 0x12. This is different from the I^2C address of the device as seen on the slave I^2C controller by the applications processor. The I^2C address of the ICM-20602 is 0x68 or 0x69 depending upon the value driven on AD0 pin.

9.44 REGISTERS 119, 120, 122, 123, 125, 126 – ACCELEROMETER OFFSET REGISTERS

Register Name: XA_OFFSET_H
Register Type: READ/WRITE
Register Address: 119 (Decimal); 77 (Hex)

BIT	NAME	FUNCTION
[7:0]	XA_OFFS[14:7]	Upper bits of the X accelerometer offset cancellation. ±16g Offset cancellation in all Full Scale modes, 15 bit 0.98-mg steps

Register Name: XA_OFFSET_L
Register Type: READ/WRITE
Register Address: 120 (Decimal); 78 (Hex)

BIT	NAME	FUNCTION
[7:1]	XA_OFFS[6:0]	Lower bits of the X accelerometer offset cancellation. ±16g Offset cancellation in all Full Scale modes, 15 bit 0.98-mg steps
[0]	-	Reserved.

Register Name: YA_OFFSET_H
Register Type: READ/WRITE
Register Address: 122 (Decimal); 7A (Hex)

BIT	NAME	FUNCTION
[7:0]	YA_OFFS[14:7]	Upper bits of the Y accelerometer offset cancellation. ±16g Offset cancellation in all Full Scale modes, 15 bit 0.98-mg steps

Register Name: YA_OFFSET_L
Register Type: READ/WRITE
Register Address: 123 (Decimal); 7B (Hex)

BIT	NAME	FUNCTION
[7:1]	YA_OFFS[6:0]	Lower bits of the Y accelerometer offset cancellation. ±16g Offset cancellation in all Full Scale modes, 15 bit 0.98-mg steps
[0]	-	Reserved.

Register Name: ZA_OFFSET_H
Register Type: READ/WRITE
Register Address: 125 (Decimal); 7D (Hex)

BIT	NAME	FUNCTION
[7:0]	ZA_OFFS[14:7]	Upper bits of the Z accelerometer offset cancellation. ±16g Offset cancellation in all Full Scale modes, 15 bit 0.98-mg steps

Register Name: ZA_OFFSET_L
Register Type: READ/WRITE
Register Address: 126 (Decimal); 7E (Hex)

BIT	NAME	FUNCTION
[7:1]	ZA_OFFS[6:0]	Lower bits of the Z accelerometer offset cancellation. ±16g Offset cancellation in all Full Scale modes, 15 bit 0.98-mg steps
[0]	-	Reserved.

10 USE NOTES

10.1 TEMPERATURE SENSOR DATA

Temperature sensor data goes into the FIFO whenever the FIFO is enabled and there is a sensor active unless the temperature is explicitly disabled.

10.2 ACCELEROMETER-ONLY LOW-NOISE MODE

The first output sample in Accelerometer-Only Low-Noise Mode after wake up from sleep always has 1 ms delay, independent of ODR.

10.3 ACCELEROMETER LOW-POWER MODE

Changing the value of SMPLRT_DIV register in Accelerometer Low-Power mode will take effect after up to one sample at the old ODR.

10.4 SENSOR MODE CHANGE

When switching from low-power modes to low-noise modes, unsettled output samples may be observed at the gyroscope or accelerometer outputs due to filter switching and settling. The number of unsettled output samples depends on the filter and ODR settings. The number of unsettled output samples is minimized by selecting the widest low-noise-mode filter bandwidth consistent with the chosen ODR.

10.5 TEMP SENSOR DURING GYROSCOPE STANDBY MODE

During transition from Gyro Low power mode (GYRO_CYCLE=1), to Gyro Standby mode, in addition to the Gyro axis (axes) being turned off, the Temp Sensor will also be turned off if the Accel is disabled. In order to keep the temp sensor on during Gyroscope standby mode when Accel is disabled, the following procedure should be followed:

- Set GYRO_CYCLE = 0 at least one ODR cycle prior to entering Standby mode
- At least one of the Gyro axis is ON prior to entering Standby mode
- Set GYRO_STANDBY = 1

10.6 GYROSCOPE MODE CHANGE

Gyroscope will take one ODR clock period to switch from Low-Noise to Low-Power mode after GYRO_CYCLE bit is set.
If GYRO_CYCLE is set to 1 prior to turning on the gyroscope, the first sample will be from low-noise mode, which may not be a settled value. It is therefore recommended to ignore the first reading in this case.

10.7 POWER MANAGEMENT 1 REGISTER SETTING

It is required to set CLKSEL[2:0] to 001 (auto-select) for full performance.

10.8 UNLISTED REGISTER LOCATIONS

Do not read unlisted register locations in Sleep mode as this may cause the device to hang up, requiring power cycle to restore operation.

10.9 CLOCK TRANSITION WHEN GYROSCOPE IS TURNED OFF

When the gyroscope is on, the on-chip master clock source will be the gyroscope clock (assuming CLKSEL[2:0] = 001 for auto-select mode); otherwise, the master clock source will be the internal oscillator as long as the part is not in Sleep mode. During a power mode transition, whenever the gyroscope is disabled and the part enters a mode other than Sleep, the on-chip master clock source will transition from the gyroscope clock to the internal oscillator. It will take about 20 µs for this transition to complete.

10.10 SLEEP MODE

The part will only enter Sleep mode when the SLEEP bit in PWR_MGMT_2 is set to '1'. If SLEEP bit is '0' and bit STBY_[X,Y,Z]A and STBY_[X,Y,Z]G are all set to '1', accelerometer and gyroscope will be turned off, but the on-chip master clock will still be running and consuming power.

10.11 NO SPECIAL OPERATION NEEDED FOR FIFO READ IN LOW POWER MODE

The use of FIFO is enabled in all modes including low power mode.

10.12 GYROSCOPE STANDBY PROCEDURE

The follow precaution and procedure must be followed while using the Gyroscope Standby mode:

Precaution to follow while entering Standby Mode:

- The user will ensure that at least one gyro axis is ON when setting gyro_standby = 1.

Procedure to transition from Gyro Standby to Gyro off:

- The user should set gyro_standby = 0 first
- Next, turn off gyro x/y/z.

11 ASSEMBLY

This section provides general guidelines for assembling TDK-InvenSense Micro Electro-Mechanical Systems (MEMS) gyros packaged in LGA package.

11.1 ORIENTATION OF AXES

The diagram below shows the orientation of the axes of sensitivity and the polarity of rotation. Note the pin 1 identifier (•) in the Figure 13.

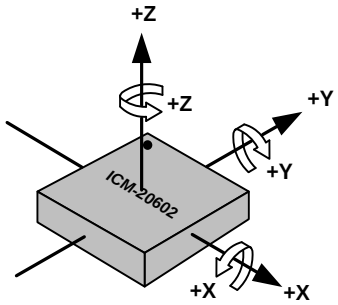


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Figure 13. Orientation of Axes of Sensitivity and Polarity of Rotation

12.1 PACKAGE DIMENSIONS

16 Lead LGA (3x3x0.75) mm NiAu pad finish

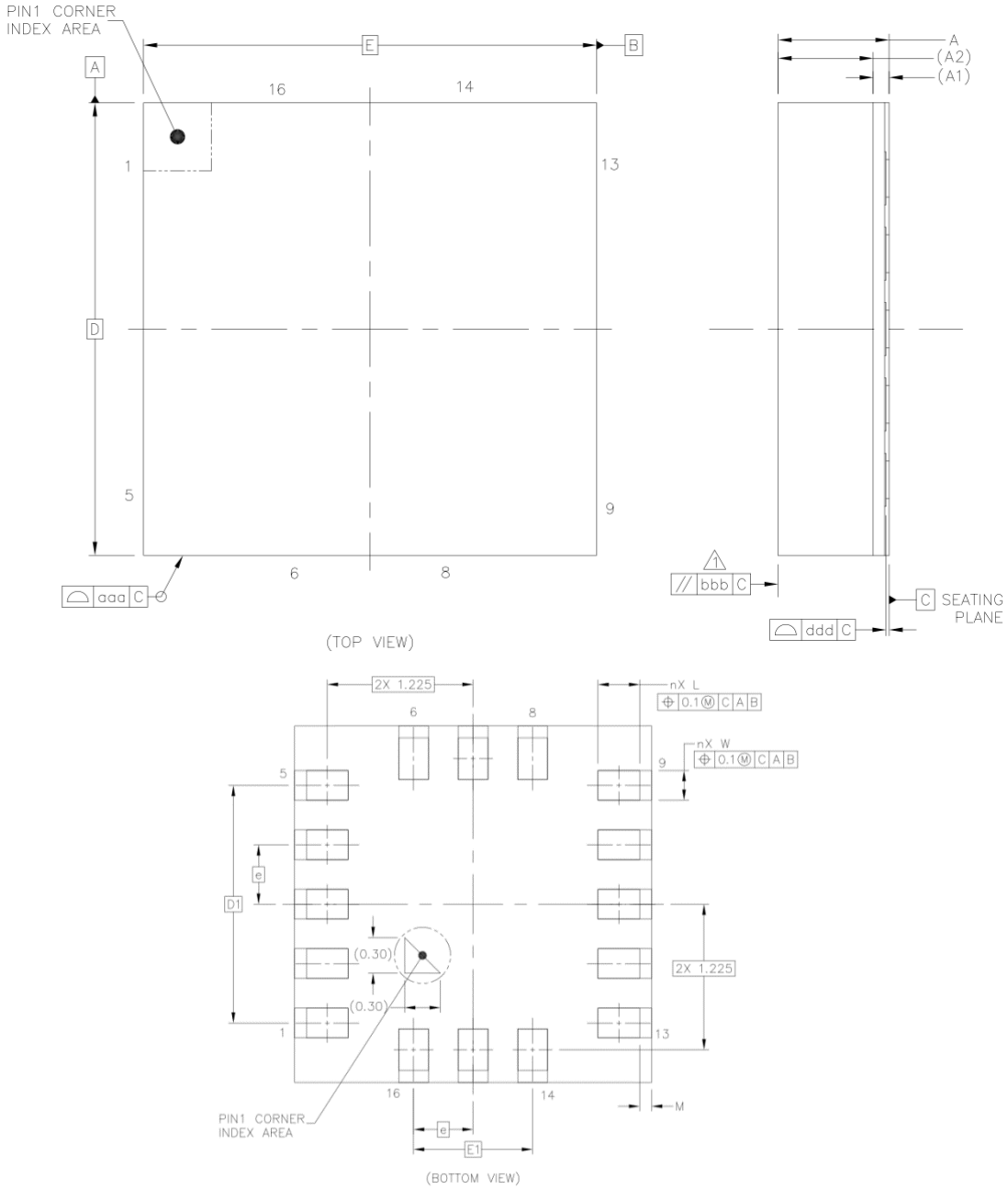

Figure 14. Package Dimensions

	SYMBOLS	DIMENSIONS IN MILLIMETERS		
		MIN	NOM	MAX
Total Thickness	A	0.7	0.75	0.8
Substrate Thickness	A1		0.105 REF	
Mold Thickness	A2		0.63 REF	
Body Size	D	2.9	3	3.1
	E	2.9	3	3.1
Lead Width	W	0.2	0.25	0.3
Lead Length	L	0.3	0.35	0.4
Lead Pitch	e		0.5 BSC	
Lead Count	n		16	
Edge Ball Center to Center	D1		2 BSC	
	E1		1 BSC	
Body Center to Contact Ball	SD		---	
	SE		---	
Ball Width	b	---	---	---
Ball Diameter			---	
Ball Opening			---	
Ball Pitch	e1		---	
Ball Count	n1		---	
Pre-Solder		---	---	---
Package Edge Tolerance	aaa		0.1	
Mold Flatness	bbb		0.2	
Coplanarity	ddd		0.08	
Ball Offset (Package)	eee		---	
Ball Offset (Ball)	fff		---	
Lead Edge to Package Edge	M	0.05	0.1	0.15

Table 16. Package Dimensions Table

13 PART NUMBER PACKAGE MARKING

The part number package marking for ICM-20608 devices is summarized below:

PART NUMBER	PART NUMBER PACKAGE MARKING
ICM-20602	I62

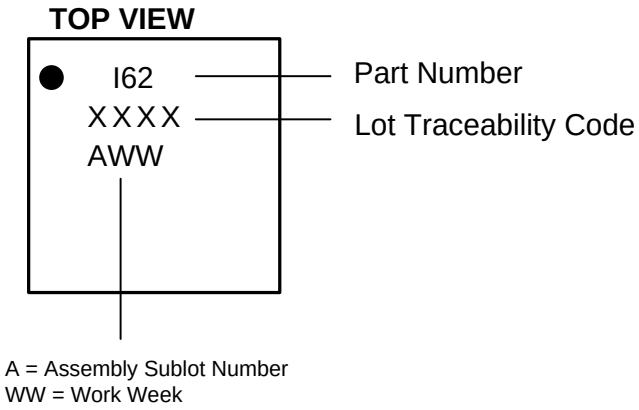

Figure 15. Part Number Package Marking

14 REVISION HISTORY

REVISION DATE	REVISION	DESCRIPTION
10/03/2016	1.0	Initial Release
06/27/2018	1.1	Updated Sections 8, 9

15 ENVIRONMENTAL COMPLIANCE

The ICM-20602 is RoHS and Green compliant. The ICM-20602 is in full environmental compliance as evidenced in report HS-ICM-20602A, Materials Declaration Data Sheet.

Environmental Declaration Disclaimer:
InvenSense believes this environmental information to be correct but cannot guarantee accuracy or completeness. Conformity documents for the above component constitutes are on file. InvenSense subcontracts manufacturing and the information contained herein is based on data received from vendors and suppliers, which has not been validated by InvenSense.

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