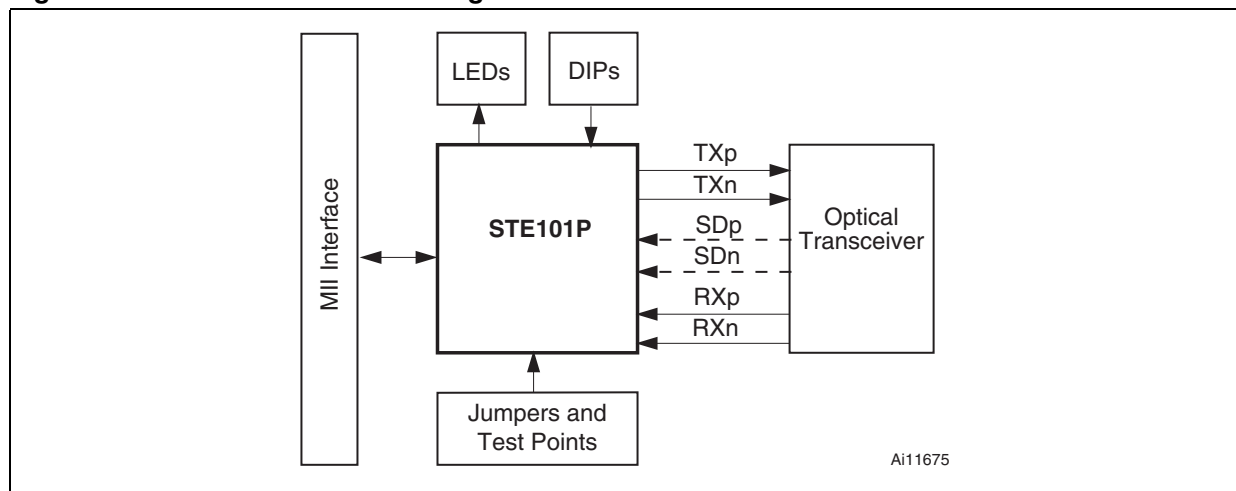


STE101P Reference Design Board for 100Base-FX, 100Base-TX and 10Base-T

Introduction

The STE101P Reference Design Board lets you get started developing 100Base-FX, 100Base-TX and 10Base-T applications for the STE101P Fast Ethernet physical layer (PHY) interface. It provides a Media Independent Interface (MII) for easy attachment to a 10/100 Media Access Controllers (MAC) and a physical media interface for 100Base-FX, 100Base-TX and 10Base-T. Many switches, jumpers and test points make it easy to evaluate all the features provided by the STE101P transceiver.

Figure 1. STE101P Reference Design Board Overview



Main features of STE101P Transceiver

- 3.3V low power operation
- Operates either in full duplex or half duplex, provides loop-back modes for diagnostic testing
- MII, RMII, and SMII interfaces supported
- Auto crossover / polarity (auto-MDIX) feature
- Provides auto-negotiation (T, TX modes), parallel detection or manual control for mode setting

Main features of STE101P Reference Design Board for 100Base-FX

- Uses 5V power supply either from MII connector or test point
- 16 jumpers and 14 test points for evaluating and testing all PHY modes such as MDint, Mdix, Rip, SMII, RMII, PHY address and power consumption measurement
- Hardware control pins set the initial state of the STE101P at power-up
- Entire MII is highlighted by both a standard industrial connector and easy-to-use scope lock-on header
- 6 LEDs indicate: power supply, speed, duplex mode, Tx/Rx activity and link status

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1 General information

Designed to be directly connected to the standard industrial Media Independent Interface (MII) connector of a Media Access Controller (MAC) layer, the STE101P Reference Design Board enables the evaluation and use of the STE101P 10/100 Fast Ethernet 3.3V Transceiver in 100Base-FX, 100Base-TX and 10Base-T applications and provides useful information for hardware designers on how to improve application performance.

1.1 Test environment

For getting started and additional testing the design of your application, the following test environment and test machines can be used:

- STE10/100A PCI Ethernet card with outgoing MII interface of its MAC layer. For more details about the product and reference design board, please refer to application note *AN1302: STE10/100A - PCI 10/100 Ethernet Controller with Integrated PHY*.
- Smartbits network performance analysis system for MII connections. For more information, please refer to manufacturer documentation (www.spirentcom.com)
- Netcom X-1000, it provides MII connections. For more information, please refer to manufacturer documentation.

1.2 Board setup

Figure 2 shows the top silkscreen of the STE101P Reference Design Board. Black squares represent jumpers and gray circles represent test points.

Section 2: Design and layout guidelines includes photos of assemblies for both FX and TX modes.

Figure 2. STE101P Reference Design Board Layout

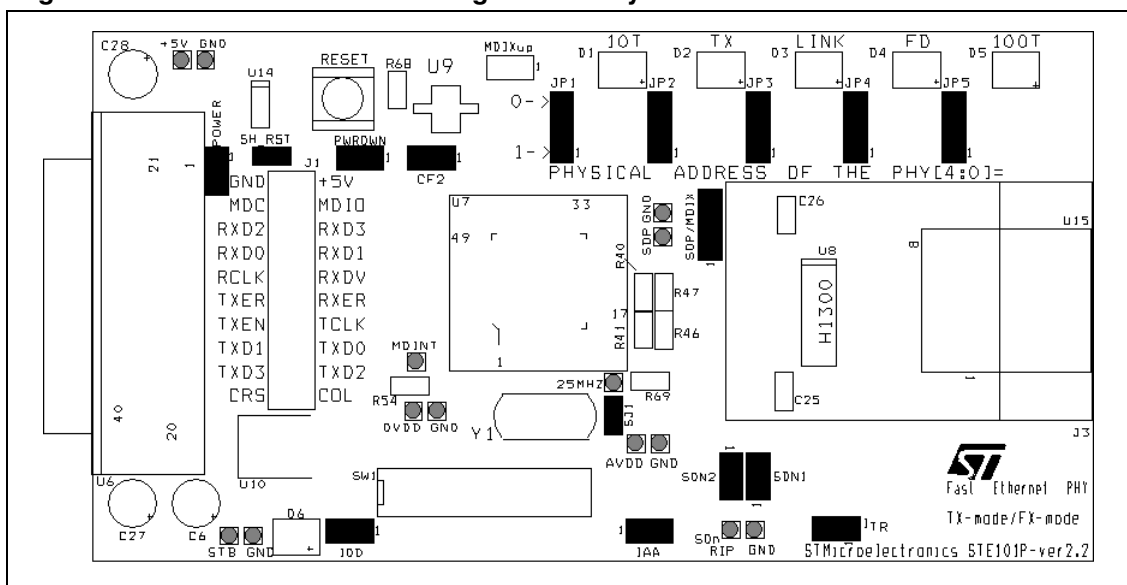


Figure 3. STE101P Reference Design Board in FX mode

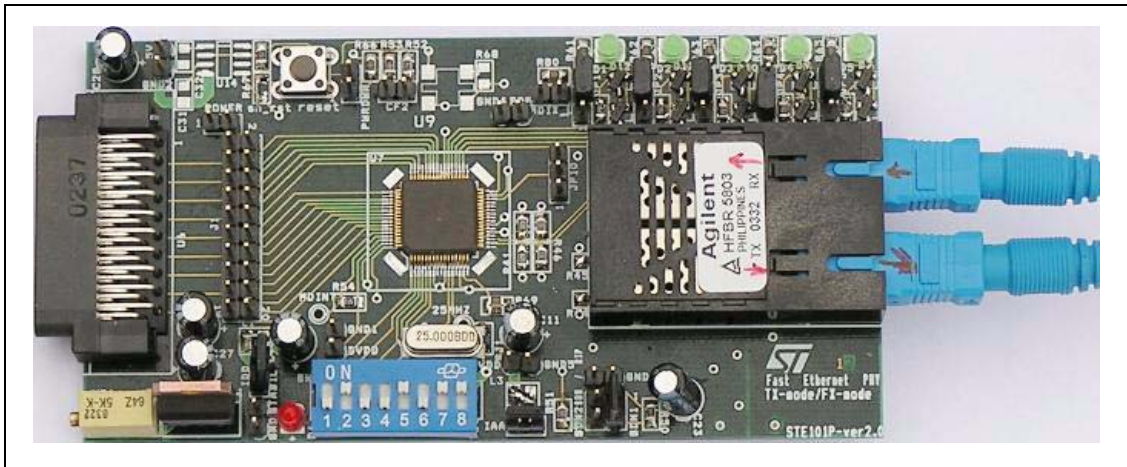
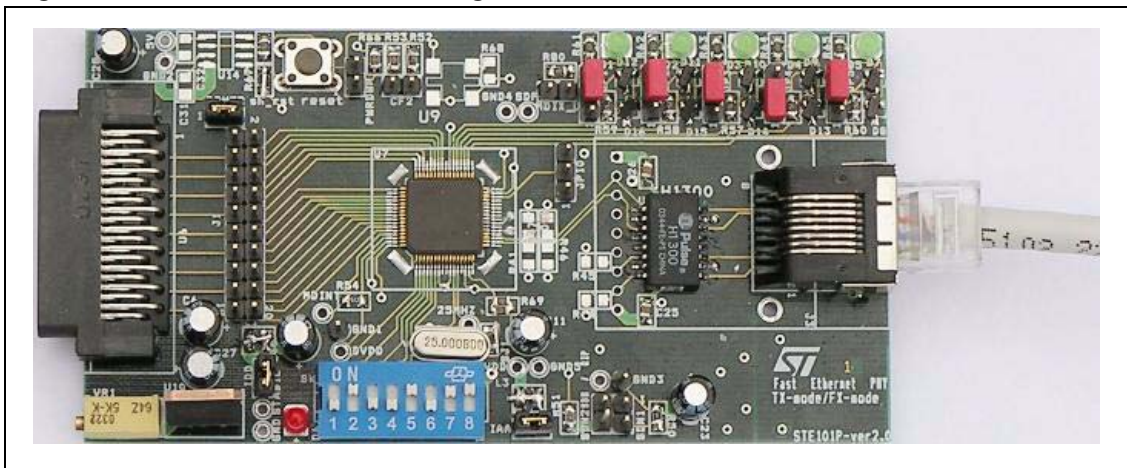


Figure 4. STE101P Reference Design Board in TX mode



1.2.1 Test points

Table 1. Test Points

Test point	Description	Location
+5V	+5V board power supply	Upper left
STB	Stabilized 3.3V (STAB3.3V) supply immediately delivered from +5V	Lower left
DVDD	Decoupled STAB3.3V for digital power supply of the STE101P	Lower left
AVDD	Decoupled STAB3.3V for analogue power supply of the STE101P	Lower middle
GND	Common ground of entire board, 6 locations	6 diff. locations
MDint	Manager Data interrupt	Lower left
SDp	Signal Detect positive	Upper middle
SDn/RIP	Signal Detect negative / Reset in progress	Lower right
25MHZ	25MHz clock signal for the STE101P	Lower middle
J1	Second terminal of the Media Independent Interface(MII)	Middle left

1.2.2 Jumpers

In the following tables, the term "Closed" means that both terminals of the jumper are inter-connected. In other words, the jumper is placed on the terminals on the design board.

Table 2. Jumpers (both TX and FX modes)

Jumper	Description	Default	Location
POWER	Disconnects supply from the second MII connector J1	Closed	Upper left
PWRDWN	Open: Device remains in normal power mode Closed: Switches devices into Powerdown mode	Open	Upper left
SH_RST	Open: Reset/Supply Supervision circuit enabled Closed: By-passes Reset/Supply Supervision circuit ⁽¹⁾	Closed	Upper left
CF2	Open: Standard MII features are enabled Closed: RMII and SMII features are enabled	Open	Upper left
JP1 to 5	PHY address. Address can be between 0 and 31. ⁽²⁾	2-3 Closed	Upper right
SJ1	Open: On-board crystal disconnected from the STE101P. ⁽³⁾ Closed: On-board crystal connected to the STE101P	Closed	Lower middle
IDD	Open: Used to measure power consumption of Digital part Closed: Bypasses 1-Ohm resistor in the DVDD line ⁽⁴⁾	Closed	Lower left
IAA	Open: Used to measure power consumption of Analog part Closed: Bypasses 1-Ohm resistor in the AVDD line ⁽⁴⁾	Closed	Lower middle

1. Must be closed if the Reset/Supply Supervision circuit (optional) is not present.
2. JP1 to 5 represent the PHY address [4:0]. When pins 2 and 3 are connected (closed), the PHY address bit will be set to 0. JP5 is the LSB and JP1 is the MSB bit of the PHY address. Default value is 00000.
3. When using an external clock, jumper SJ1 must be left open and the external clock connected to the 25-MHz test point.

4. Each terminal of the IDD jumper are connected to one end of the 1-Ohm SMD resistor. If the jumper is left open, the voltage drop on the resistor can be measured between two terminals of the jumper. The measured voltage drop represents the power consumption of the digital part of the chip STE101P. The IAA jumper is the same, therefore the power consumption of the analog part of the chip STE101P can also be measured. When not measuring the power consumption, close the jumpers to prevent increased noise on the supply lines.

Table 3. Jumpers (FX mode only)

Jumper	Description	Default	Location
SDP/MDIX	If pins 1 and 2 are closed, SDp signal from optical transceiver is enabled. (Pin 30 of STE101P) ⁽⁵⁾	1-2 closed	Upper middle
MDIXup	Open: Auto MDI/MDIX function enabled Closed: Auto MDI/MDIX function disabled	Closed	Upper middle
SDN1 SDN2	If the both pins are closed, the 1.27V supply is delivered to the pin SDn of the STE101P. R78 is not assembled.	Both closed	Lower right

5. Auto MDI/MDIX feature is not available in FX mode.

Table 4. Jumpers (TX mode only)

Jumper	Description	Default	Location
SDP/MDIX	If pins 2 and 3 are closed, MDIXup feature is enabled. ⁽⁶⁾	2-3 closed	Upper middle
MDIXup	Open: Auto MDI/MDIX function enabled Closed: Auto MDI/MDIX function disabled	Open	Upper middle
SDN1 SDN2	If both pins are open and R78 is assembled, the Reset In Progress (RIP) signal can be observed on the SDN/RIP test point.	Both open	Lower right

6. Auto MDI/MDIX feature is available in TX mode. (MDIXup must be open.)

1.2.3 Switches

[Table 5](#) lists the switch settings used to configure the initial state of the STE101P at power-up.

Table 5. DIP switch settings

Switch	Description	Default
1 - MF4	10/100 Mbps Speed Select Off : 100Base-T operation; On: 10Base-T operation ⁽⁷⁾	Off
2 - MF3	Enable Scrambler Off: Scrambler disabled On: Scrambler enabled	On
3 - MF2	Enable 4B/5B Coding Off: 4B/5B disabled On: 4B/5B enabled	Off
4 - MF1	Enable NRZ/NRZI Conversion Off: NRZI disabled On: NRZI enabled	Off
5 - MF0	Auto-negotiation Disable Off: Auto-negotiation enabled On: Auto-negotiation disabled	Off

Table 5. DIP switch settings (continued)

Switch	Description	Default
6 - FDE	Duplex mode Off: Full duplex; On: Half Duplex ^{(7) (8)}	Off
7 - CFG1	Loop-back Disable Off: Loop-back enabled On: Loop-back disabled ⁽⁸⁾	On
8 - CFG0	MLT3 Encoder/Decoder Enable Off: MLT3 disabled On: MLT3 enabled ⁽⁸⁾	On

7. Auto-negotiation enabled (MF0 = Off) takes precedence over MF4 and FDE settings.

8. If Auto-negotiation is enabled (MF0 = Off), use pin value described in [Table 6](#).

[Table 6](#) describes the default Auto-negotiation settings (10/100 Mbps speed and Full- or Half-Duplex modes).

Table 6. Auto-negotiation parameter settings

Device advertises	SW1 Position 5	SW1 Position 6	SW1 Position 7	SW1 Position 8
10HD	Off	On	Off	On
10HD	Off	Off	Off	On
100HD	Off	On	On	Off
100HD/FD	Off	Off	On	Off
10/100HD	Off	On	Off	Off
All	Off	Off	Off	Off

1.2.4 LEDs

[Table 7](#) describes the meaning of the various LEDs. For alternative LED solutions, please refer to [Section 2: Design and layout guidelines](#). For a more detailed description of the LED signals, please refer to the STE101P datasheet.

Table 7. LED Descriptions

LED	Description	Location
D1	10/100 Mbps Speed Detect Off: 10 Mbps operation speed is detected. On: 100 Mbps operation speed is detected.	Upper right
D2	Receive LED: Blinks at 10 Hz when receiving (no collisions detected).	Upper right
D3	Transmit LED: Blinks at 10 Hz when transmitting (no collisions detected).	Upper right
D4	Link LED: On when 100Mbps or 10Mbps link is active. It will also blink at 10 Hz for Transmit and Receive activity if bit 9 of STE101P register PR1B (0x1b) is 0 (default). It will not blink if register PR1B bit 9 = 1.	Upper right
D5	Collision LED: Blinks at 20 Hz when a collision is detected.	Upper right
D6	Power Supply Detect: On when power supply is connected to board.	Lower left

2 Design and layout guidelines

For a detailed description of the STE101P in FX mode, please refer to Application Note AN2231: *Evaluating the use of the STE101P Transceiver in FX mode in Fast Ethernet Physical Layer interfaces*. AN2231 also includes a description of the STE101P signals, voltage levels and power consumption values.

For a detailed description of the STE101P in TX mode, please refer to Application Note AN1301: *STE100P - Single Port Fast Ethernet Transceiver*. Application Note AN1301 also describes the common design guidelines for the Ethernet interface (Section 3) and crystal oscillator requirements (Section 5).

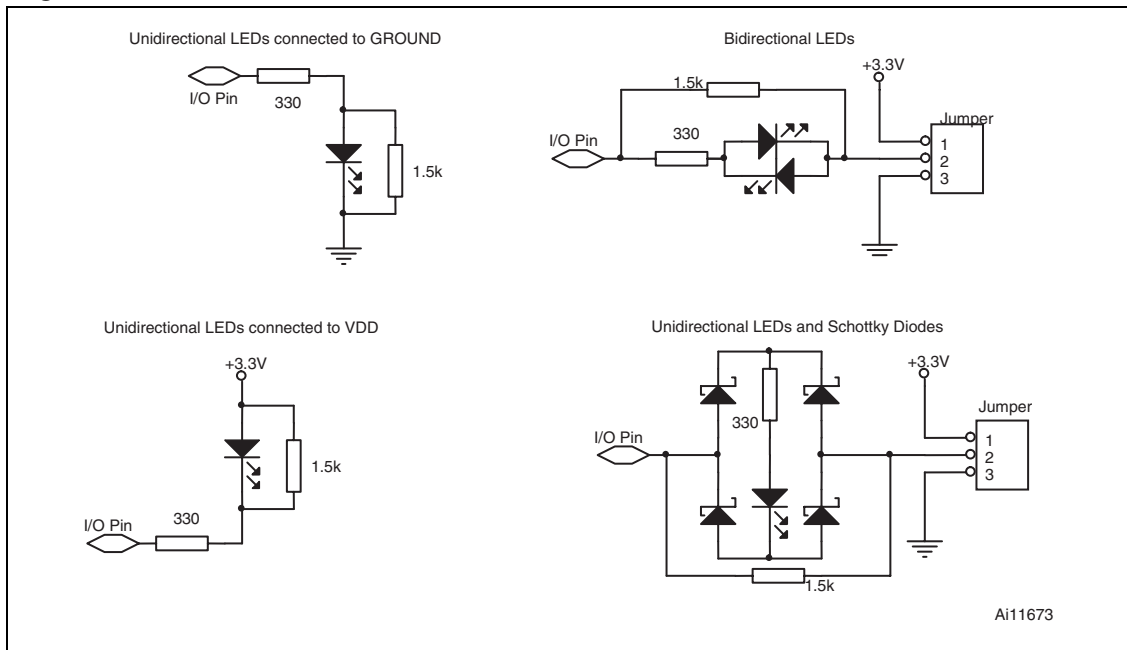
Please follow optical transceiver manufacturer recommendations when designing the power decoupling and termination circuits.

The I/O pins that set the PHY addresses are used as outputs after the reset operation. Both hardware and software reset includes the re-evaluation of all hardware-configurable registers. Logic levels on several of these pins are detected during the hardware reset period to determine their initial function. When multiplexed with LED outputs, these pins should be weakly pulled up or weakly pulled down through resistors as shown in [Figure 5](#).

2.1 LED connections

There are at least four possible ways to connect the signal LEDs. Each of the four solutions has its advantages, disadvantages and a different quantity of passive components.

Figure 5. LED Connections



Remarks concerning the circuits shown in [Figure 5](#):

- The unidirectional LED connections are the simplest solutions, but the bit of PHY address must be hard wired to Logical 1 or 0.
- The bidirectional LED connection enables a flexible change of the PHY address using a jumper. The disadvantage can be seen, for example, when using the dedicated diodes already integrated with a RJ-45 connector, panel, etc.
- The unidirectional LED connections with Schottky diodes solution is the most flexible solution enabling the use of a dedicated LED already integrated in an RJ-45 connector, panel, etc. Although this solution requires the highest quantity of components, a device integrating four Schottky diodes in a single package can be used to reduce the number of components.

2.2 Power supply

Power supply of the board must not exceed the total power dissipation of the on-board 3.3V voltage regulator (U10). Without an additional cooler, the regulator dissipates up to 1000 mW, enabling the entire board to consume up to 500 mA in FX mode. In TX mode, the board consumes less power, as the optical transceiver used in FX mode consumes most of the energy.

The voltage drop on the regulator in case that there are 5V ahead of and 3.3V behind the regulator is 1.7V. When the external power supply is 5V in this case, the power dissipation is 850 mW. If more than 5V is used to supply the board, excessive power dissipation may occur.

The voltage regulator includes a thermal protection that lowers the output voltage if the temperature of the package exceeds a certain threshold. For more information, refer to the voltage regulator datasheet.

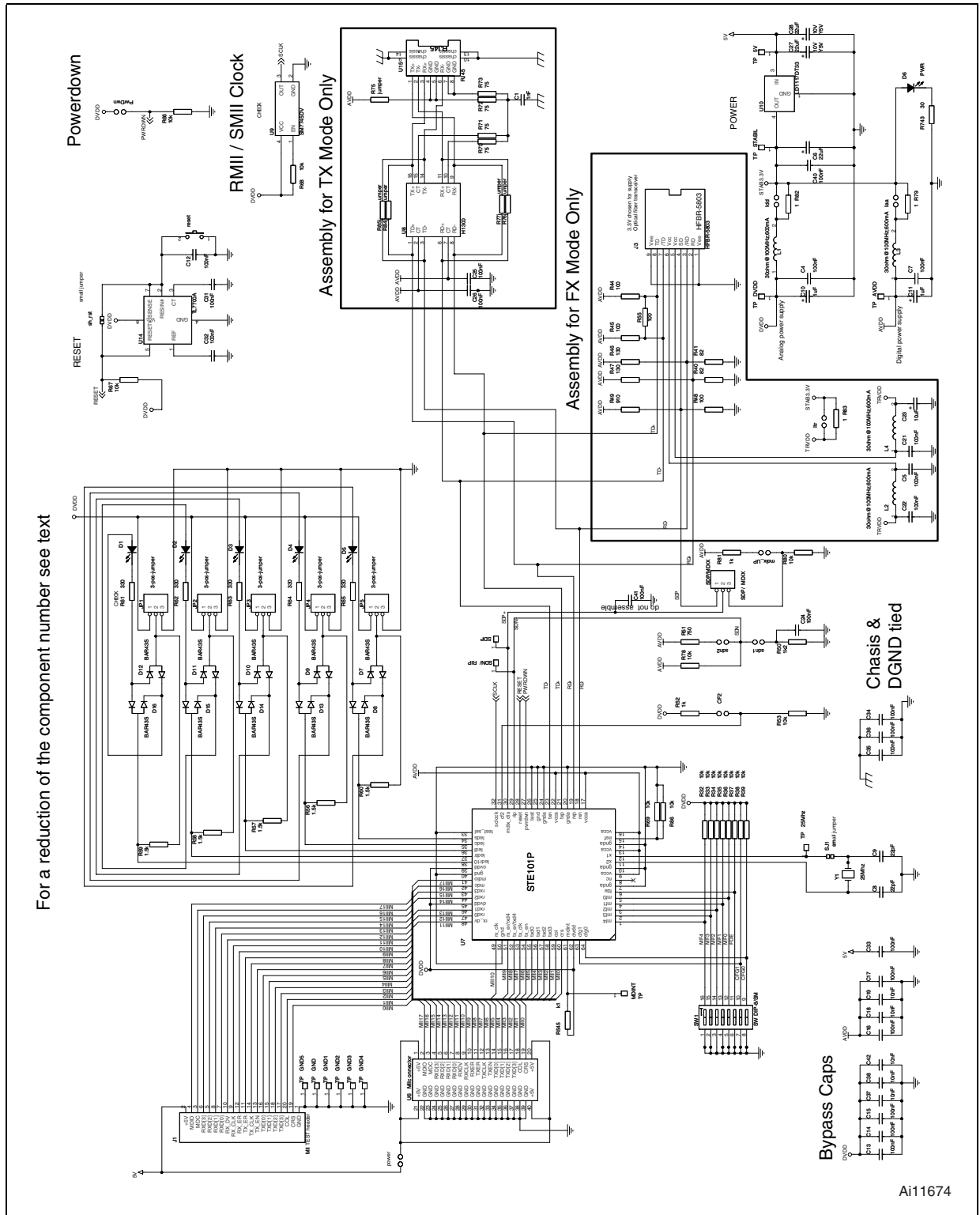
3 Typical Application

3.1 Application Diagram

Note that the polarity of the transformer is switched in [Figure 6](#). Pin TXp is connected to RDn and pin TXn is connected to RDp in order to obtain the shortest and straightest signal lines. This step reduces high-frequency radiation and improves application performance. Due to the transformer symmetry, functions are not affected.

Connect two 10k-Ohm resistors in parallel to obtain an accurate 5k-Ohm value for resistor R69.

Figure 6. Application Diagram



3.2 Bill of materials

[Table 8](#) lists the components used in the STE101P sample application shown in [Figure 6](#).

For possible component reduction, see [Section 2: Design and layout guidelines](#).

Table 8. List of components

Item	Qty.	Reference	Part	Notes
2	9	SDN1, SDN2, CF2, POWER, MDIX_UP, PWRDWN, ITR, IDD and IAA	JumperEmma	
3	1	C1	1nF	
4	22	C4, C5, C7, C12, C13, C14, C15, C16, C17, C21, C22, C24, C25, C26, C31, C32, C33, C34, C35, C36, C40 and C41	100nF	
5	3	C6, C27 and C28	22µF	
6	2	C8 and C9	22pF	
7	2	C10 and C11	1µF	
8	5	C18, C19, C37, C38 and C42	10nF	
9	1	C10 and C11	10µF	
10	5	D1, D2, D3, D4 and D5	1091QM, LED	
11	1	D6	PWR	
12	10	D7, D8, D9, D10, D11, D12, D13, D14, D15 and D16	BAR43S	
13	1	JP1	3-position jumper	
14	1	JP2	3-position jumper	
15	1	JP3	3-position jumper	
16	1	JP4	3-position jumper	
17	1	JP5	3-position jumper	
18	1	JP10	SDP / MDIX	
19	1	J1	MII TEST header	
20	1	J3	HFBR-5803 FDDI, 100Mbps ATM, and fast ethernet transceiver in low cost 1x9 package style	for FX mode only
21	2	L1 and L3	Beam	
22	2	L2 and L4	TL 0.1µH	for FX mode only
23	14	R32, R33, R34, R35, R36, R37, R38, R39, R53, R66, R67, R68, R78 and R80		
24	3	R40, R41 and R48	82, 100	
25	3	R44, R45 and R55	100	
26	3	R46, R47 and R49	130, 130, 900	
27	2	R50 and R51	1k2, 750R	

Table 8. List of components (continued)

Item	Qty.	Reference	Part	Notes
28	2	R52 and R81	1k	
29	3	R54 and R69	5k	
30	5	R56, R57, R58, R59 and R60	1.5k	
31	6	R61, R62, R63, R64, R65 and R74	330	
32	4	R70, R71, R72 and R73	75	
33	3	R79, R82 and R83	1	
34	2	SJ1, SH_RST, R76, R77, R84 and R85	small jumper	integrated transformer used
35	1	SW1	DIP-8/SM Switch	
36	1	U6	MII connector	
37	1	U7	STE101P	
38	1	U8	H1300	for TX mode only
39	1	U9	SM7745DV	optional
40	1	U10	LD1117DT33	Voltage Regulator
41	1	U14	TL7700A	optional
42	1	U15	RJ45	for TX mode only
43	1	Y1	22 MHz	
44	1	Reset	Button	

4 Revision history

Date	Revision	Changes
5-Oct-2005	1	First release.

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