

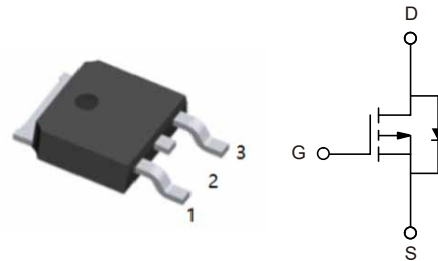
1.Description

The AOD403 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and low gate resistance. With the excellent thermal resistance of the TO-252 package, this device is well suited for high current load applications.

3.Pinning information

Pin	Symbol	Description
1	G	GATE
2	D	DRAIN
3	S	SOURCE

TO-252(DPAK)
top view



4.Absolute Maximum Ratings $T_A = 25^\circ\text{C}$

Parameter		Symbol	Rating	Units
Drain-Source Voltage		V_{DS}	-30	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current ^G	$T_C = 25^\circ\text{C}$	I_D	-70	A
	$T_C = 100^\circ\text{C}$		-55	
Pulsed Drain Current ^C		I_{DM}	-200	
Continuous Drain Current	$T_A = 25^\circ\text{C}$	I_{DSM}	-15	
	$T_A = 70^\circ\text{C}$		-12	
Avalanche Current ^C		I_{AS}, I_{AR}	-50	mJ
Avalanche energy $L=0.1\text{mH}$ ^C		E_{AS}, E_{AR}	125	
Power Dissipation ^B	$T_C = 25^\circ\text{C}$	P_D	90	W
	$T_C = 100^\circ\text{C}$		45	
Power Dissipation ^A	$T_A = 25^\circ\text{C}$	P_{DSM}	2.5	
	$T_A = 70^\circ\text{C}$		1.6	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 175	$^\circ\text{C}$



5.Thermal Characteristics

Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	t ≤ 10s	R _{θJA}	16	20	°C/W
Maximum Junction-to-Ambient ^{AD}	Steady-State		41	50	°C/W
Maximum Junction-to-Case	Steady-State	R _{θJC}	0.9	1.6	°C/W



6. Electrical Characteristic (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Drain-Source Breakdown Voltage	BV _{DSS}	I _D =-250μA, V _{GS} =0V	-30			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-30V, V _{GS} =0V			-1	μA
		T _J =55°C			-5	μA
Gate-Body leakage current	I _{GSS}	V _{DS} =0V, V _{GS} =±25V			±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =-250μA	-1.5	-2.5	-3.5	V
On state drain current	I _{D(ON)}	V _{GS} =-10V, V _{DS} =-5V	-200			A
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} =-20V, I _D =-20A, TO252		5.1	6.2	mΩ
		V _{GS} =-10V, I _D =-20A, TO252		6.2	8	mΩ
Forward Transconductance	g _{FS}	V _{DS} =-5V, I _D =-20A		42		S
Diode Forward Voltage	V _{SD}	I _S =-1A, V _{GS} =0V		-0.7	-1	V
Maximum Body-Diode Continuous Current ^G	I _S				-70	A
Input Capacitance	C _{iss}	V _{GS} =0V, V _{DS} =-15V, f=1MHz	2310	2890	3500	pF
Output Capacitance	C _{oss}		410	585	760	pF
Reverse Transfer Capacitance	C _{rss}		280	470	660	pF
Gate resistance	R _g	V _{GS} =0V, V _{DS} =0V, f=1MHz	1.9	3.8	5.7	Ω
Total Gate Charge	Q _g	V _{GS} =-10V, V _{DS} =-15V I _D =-20A				nC
Gate Source Charge	Q _{gs}		10	12	14	nC
Gate Drain Charge	Q _{gd}		10	16	22	nC
Turn-On DelayTime	t _{D(on)}	V _{GS} =-10V, V _{DS} =-15V R _L =0.75Ω, R _{GEN} =3Ω		16		ns
Turn-On Rise Time	t _r			12		ns
Turn-Off DelayTime	t _{D(off)}			45		ns
Turn-Off Fall Time	t _f			22		ns
Body Diode Reverse Recovery Time	t _{rr}	I _F =-20A, dI/dt=100A/μs	14	18	22	ns
Body Diode Reverse Recovery Charge	Q _{rr}	I _F =-20A, dI/dt=100A/μs	9	11	13	nC



- A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A = 25^\circ\text{C}$. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ and the maximum allowed junction temperature of 150°C . The value in any given application depends on the user's specific board design, and the maximum temperature of 175°C may be used if the PCB allows it.
- B. The power dissipation P_D is based on $T_{J(MAX)} = 175^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
- C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)} = 175^\circ\text{C}$. Ratings are based on low frequency and duty cycles to keep initial $T_J = 25^\circ\text{C}$.
- D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.
- E. The static characteristics in Figures 1 to 6 are obtained using $<300\mu\text{s}$ pulses, duty cycle 0.5% max.
- F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)} = 175^\circ\text{C}$. The SOA curve provides a single pulse rating.
- G. The maximum current rating is package limited.
- H. These tests are performed with the device mounted on 1 in ² FR-4 board with 2oz. Copper, in a still air environment with $T_A = 25^\circ\text{C}$.



7.1 Typical characteristic

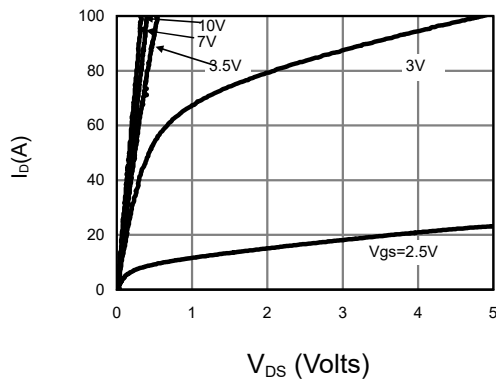


Fig 1: On-Region Characteristics (Note E)

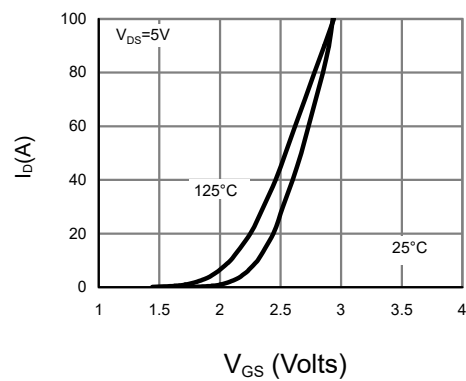


Figure 2: Transfer Characteristics (Note E)

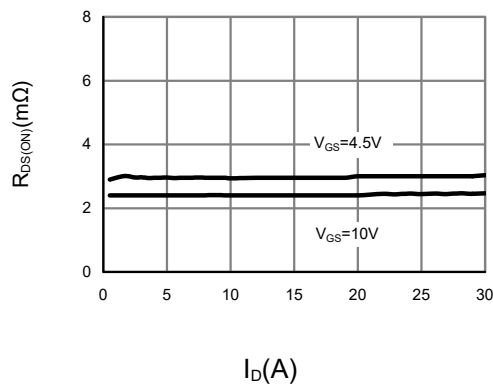


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

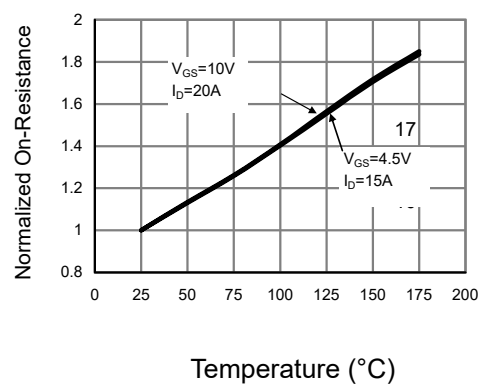


Figure 4: On-Resistance vs. Junction Temperature (Note E)

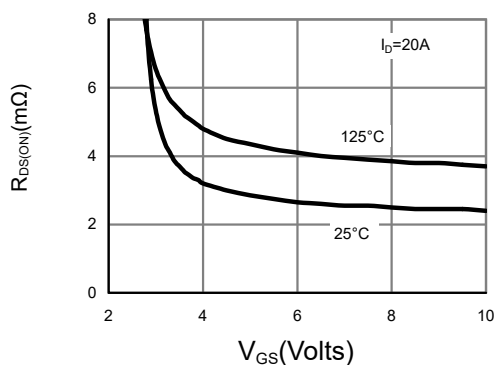


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

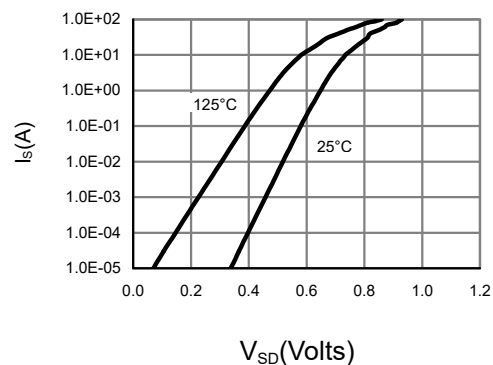


Figure 6: Body-Diode Characteristics (Note E)



7.2 Typical characteristic

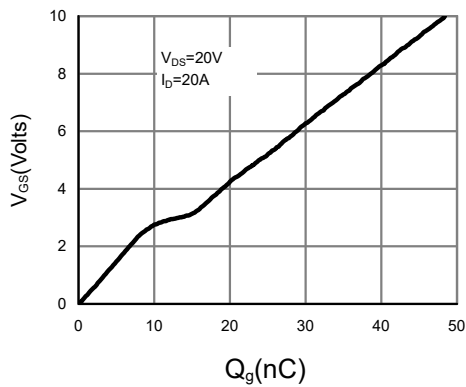


Figure 7: Gate-Charge Characteristics

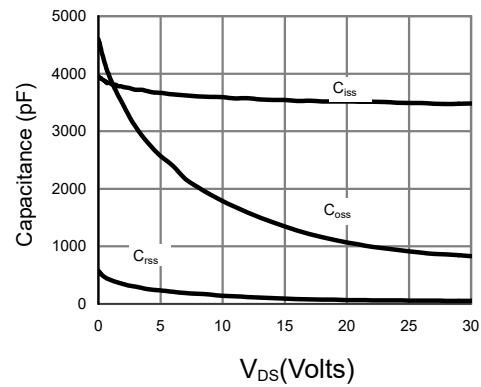


Figure 8: Capacitance Characteristics

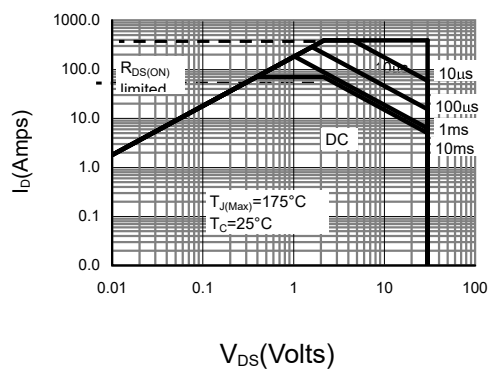


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

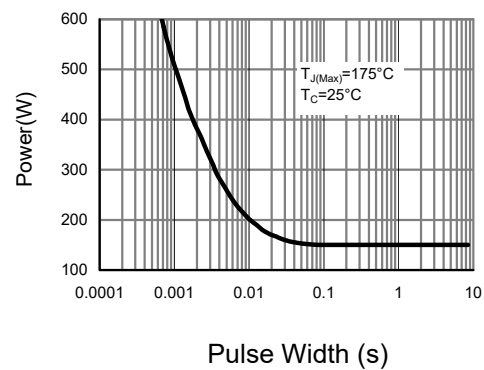


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

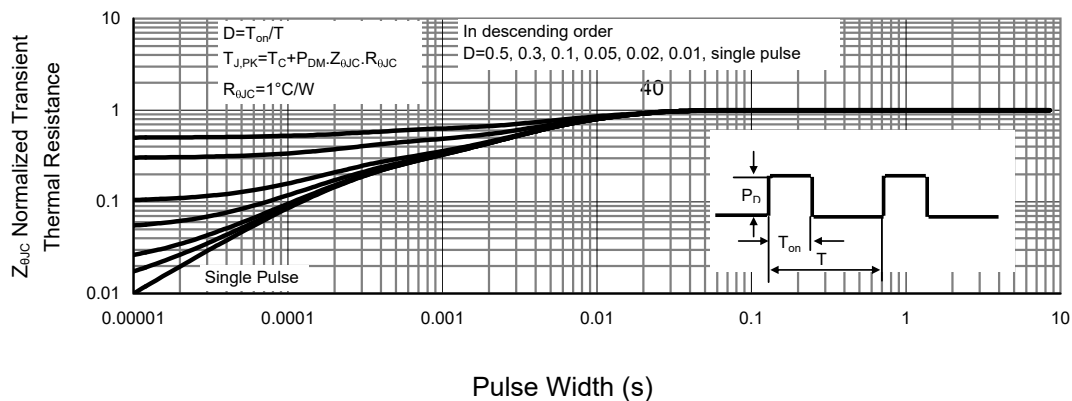


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)



7.3 Typical characteristic

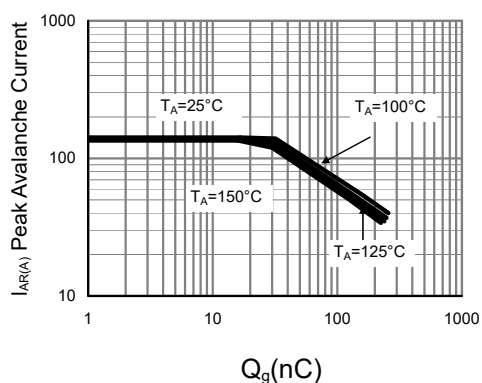


Figure 12: Gate-Charge Characteristics

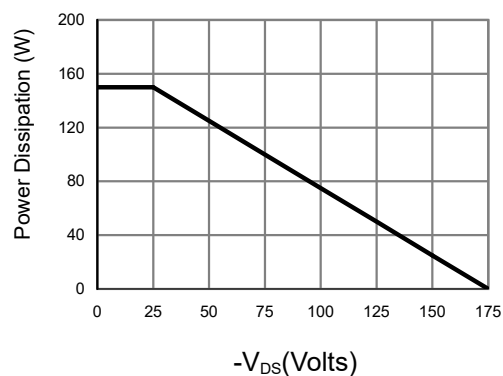


Figure 13: Capacitance Characteristics

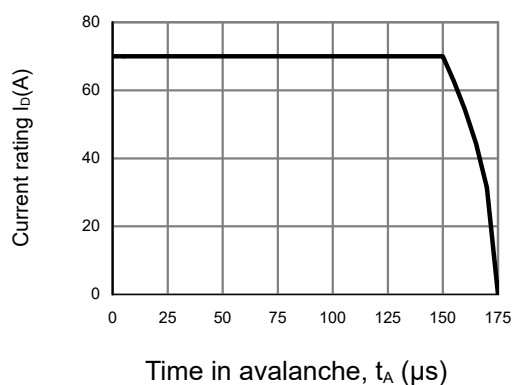


Figure 14: Single Pulse Avalanche capability (Note C)

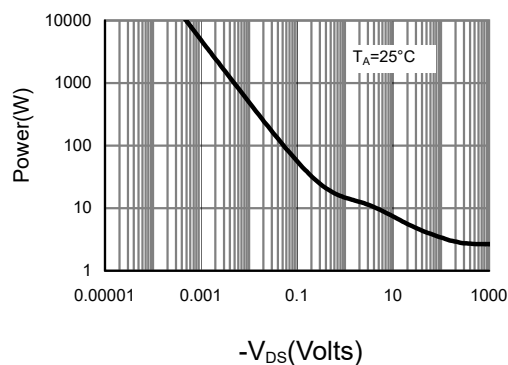


Figure 15: Maximum Forward Biased Safe Operating Area (Note F)

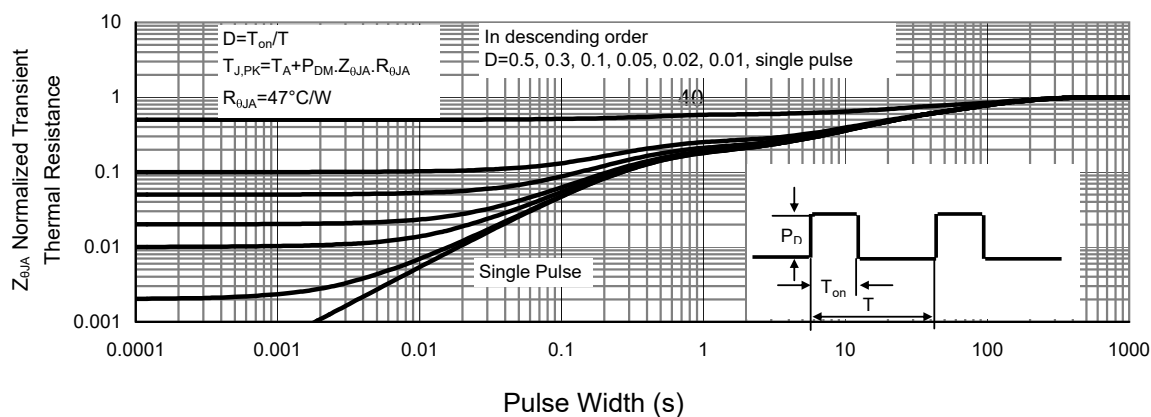
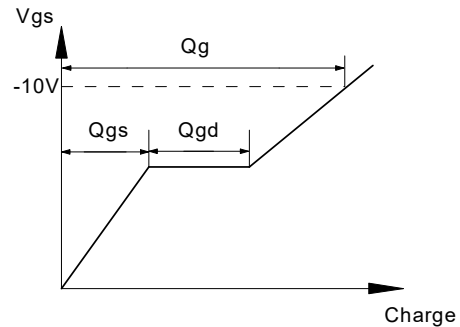
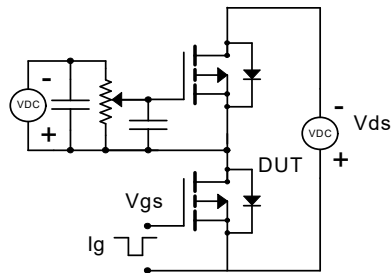


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

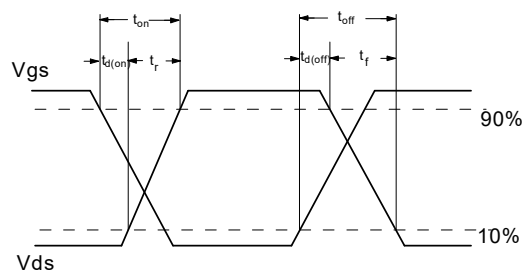
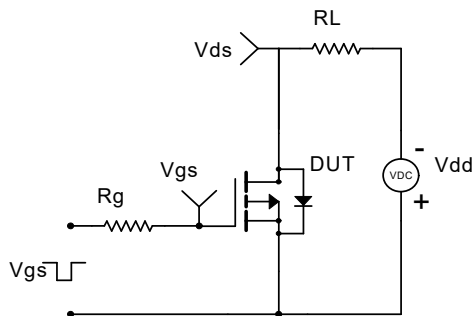


7.4 Typical characteristic

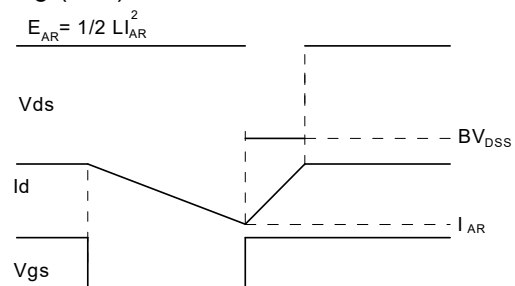
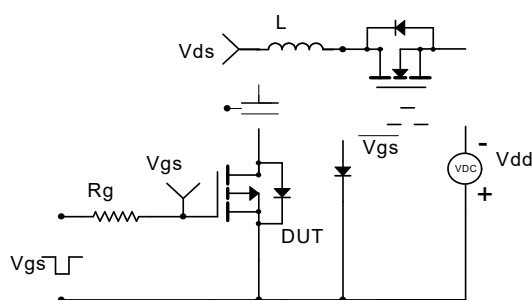
Gate Charge Test Circuit & Waveform



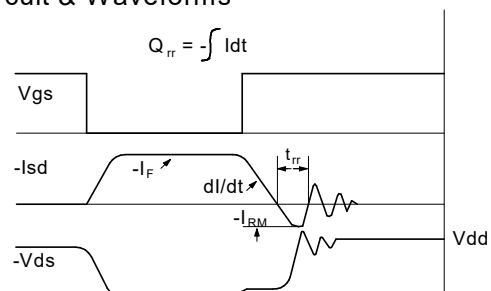
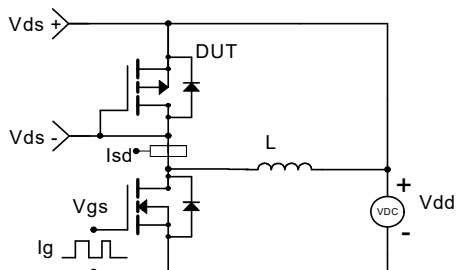
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

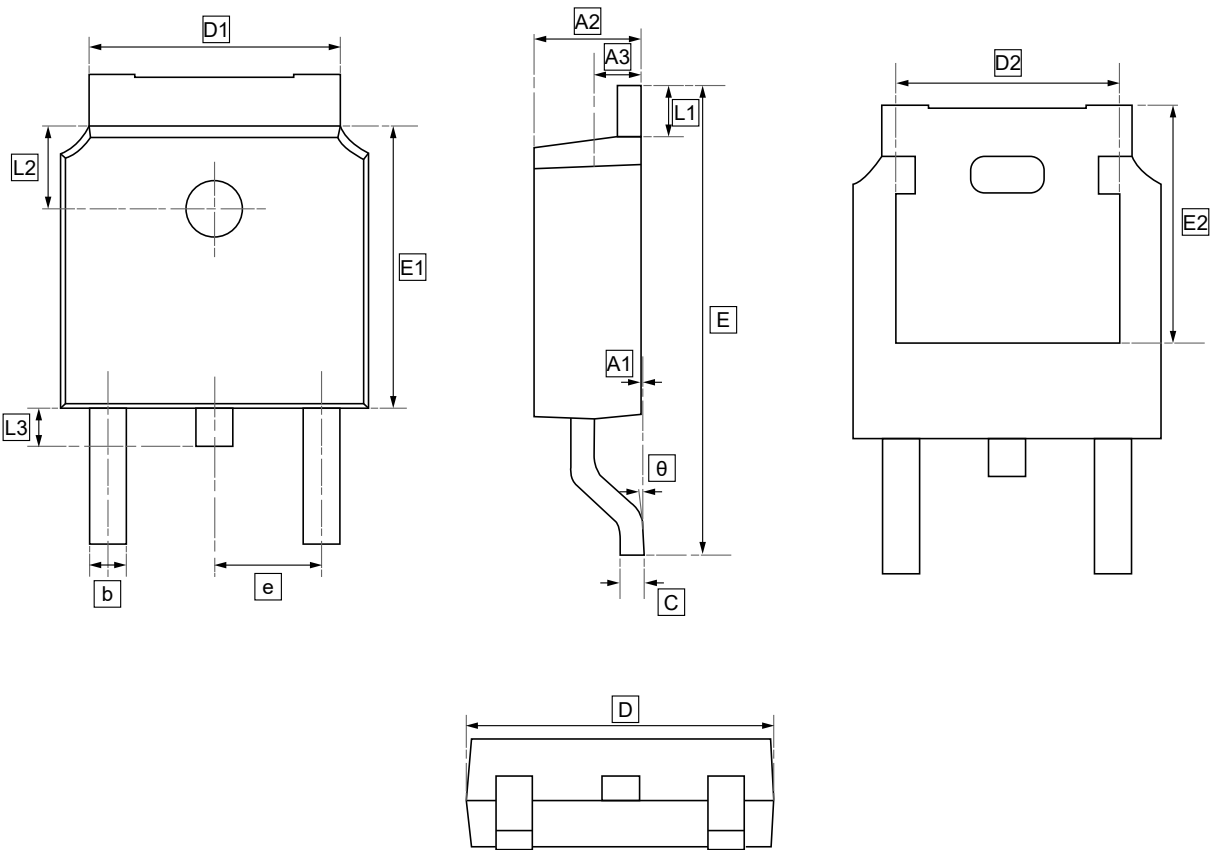


Diode Recovery Test Circuit & Waveforms





8.TO-252 Package Outline Dimensions

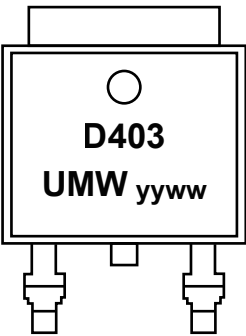


DIMENSIONS (mm are the original dimensions)

Symbol	A1	A2	A3	b	c	D	D1	D2	E	E1	E2	e	L1	L2	L3	θ
Min	0.00	2.18	0.90	0.65	0.46	6.35	4.95	4.32	9.40	5.97	5.21	2.286	0.89	1.70	0.60	0.00
Max	0.13	2.39	1.10	0.85	0.61	6.73	5.46	4.90	10.41	6.22	5.38		1.27	1.90	1.00	8.00



9.Ordering information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW AOD403	TO-252	2500	Tape and reel



10.Disclaimer

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