Soldering the QFN Stacked Die Sensors to PC Board

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INTRODUCTION

The third generation of inertial sensors (accelerometers) uses the Quad Flat No-Lead (QFN) platform with stacked die configuration to minimize the footprint. QFN sensors are the first product of its kind for Freescale Semiconductor. This application note describes suggested methods of soldering these devices to the PC board. Figure 1 shows the top and bottom view of QFN 16 lead, 6 x 6 mm individual sensor devices and the device soldered to the board.



Figure 1. QFN 16-Lead, 6x6 mm Stacked Die Sensor

Overview of Soldering Considerations

Information provided here is based on experiments executed on QFN devices. They do not represent exact conditions present at a customer site. Hence, information herein should be used as guidance and any necessary adjustments required by customers.

The stacked die QFN is designed for both commercial and automotive applications. Solder Joint Reliability (SJR) varies for both applications.

- Commercial applications require 500 temperature cycles (-40°C to +125°C).
- Automotive applications required up to 2000 temperature cycles for solder joint reliability (SJR).

To meet automotive applications, as well as severe reflow conditions like that of Sony, the exposed pad (die pad or flag) should also to be soldered to the PC board. However, it is always recommended to solder the exposed flag to the PC board, thereby increasing SJR.

Freescale QFN sensors are compliant with Restrictions on Hazardous Substances (RoHS), having halide free molding compound (green) and lead-free terminations. These terminations are compatible with tin-lead (Sn-Pb) as well as tin-silver-copper (Sn-Ag-Cu) solder paste soldering processes. Reflow profiles applicable to those processes can be used successfully for soldering the devices. This document provides a suggested reflow profile for JEDEC compliant for the lead-free soldering process as well as the footprint information for the QFN device.

Test Procedure

The test board panel design for QFN stacked die package incorporates input from customers as to thickness, trace material, and layers of construction. This was accomplished to simulate as nearly as possible, the same conditions the package will be subjected to by customers. Solder paste printing at the board level is a critical factor in solder-joint reliability for QFN and all leadless devices. The final stencil used had a thickness of 6 mils (150 microns). The I/O pad openings (for the so-called *leads*) were 1:1 with the PCB pad size. The exposed flag region for the stencil was pulled away from the I/O to reduce the likelihood for solder bridging or scavenging. Because the evaluation was to only determine the solder joints, good electrical dies were required.

Mechanical dies to simulate the actual thermal cycling conditions were used in assembly. To check for solder failure, an electrical opening was viewed as a sign. Hence, all the leads were shorted. For redundancy, two wire bonds were provided for each joint. Temperature range for the experimental cycling was from -40°C to +125°C with 15 minute dwells at extreme and 15 minute ramps between extremes. The chamber of various packages and test boards was temperature profiled for stability.

Resistance measurements through the daisy chain nets were on a continuous basis. Event detectors measured the resistance with a setup point of 300 Ω being the failure criterion [IPC-SM-785]. The start resistance for the QFN



packages through the daisy chain was on the order of 1 Ω . When the event detectors recorded a failure, the net failing was identified and documented. Results indicated the first failure (with exposed flags soldered down) was more than 2000 temperature cycles. The first failure, with Sony reflow conditions, occurred beyond 1000 cycles with exposed flag soldered down.

Footprint and Reflow Profiles

Figure 2 provides the JEDEC compliant reflow conditions.

Figure 3 illustrates the footprint of the QFN 16 lead 6 x 6 mm package for solder paste printing purposes.

Summary

There are many new applications being designed using QFN stacked die accelerometers. This document suggests soldering methods for those devices.



Figure 2. Reflow Profile for Sn-Pb and Sn-Ag-CU Solder Paste Soldering Processes



Note: The die-pad (flag) should be soldered down for automotive use. All dimensions are in mm.

Figure 3. Footprint for 16-Lead OFN, 6 x 6 mm

Sensor Device Data Freescale Semiconductor

AN3111

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