4-Mbit (512K x 8) Static RAM

Features

- **Pin- and function-compatible with CY7C1049B**
- **High speed**
  - **— t_{AA} = 10 ns**
- **Low active power**
  - **— I_{CC} = 90 mA @ 10 ns**
- **Low CMOS Standby power**
  - **— I_{SB2} = 10 mA**
- **2.0V Data Retention**
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**
- **Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features**
- **Available in lead-free 36-Lead (400-Mil) Molded SOJ package**

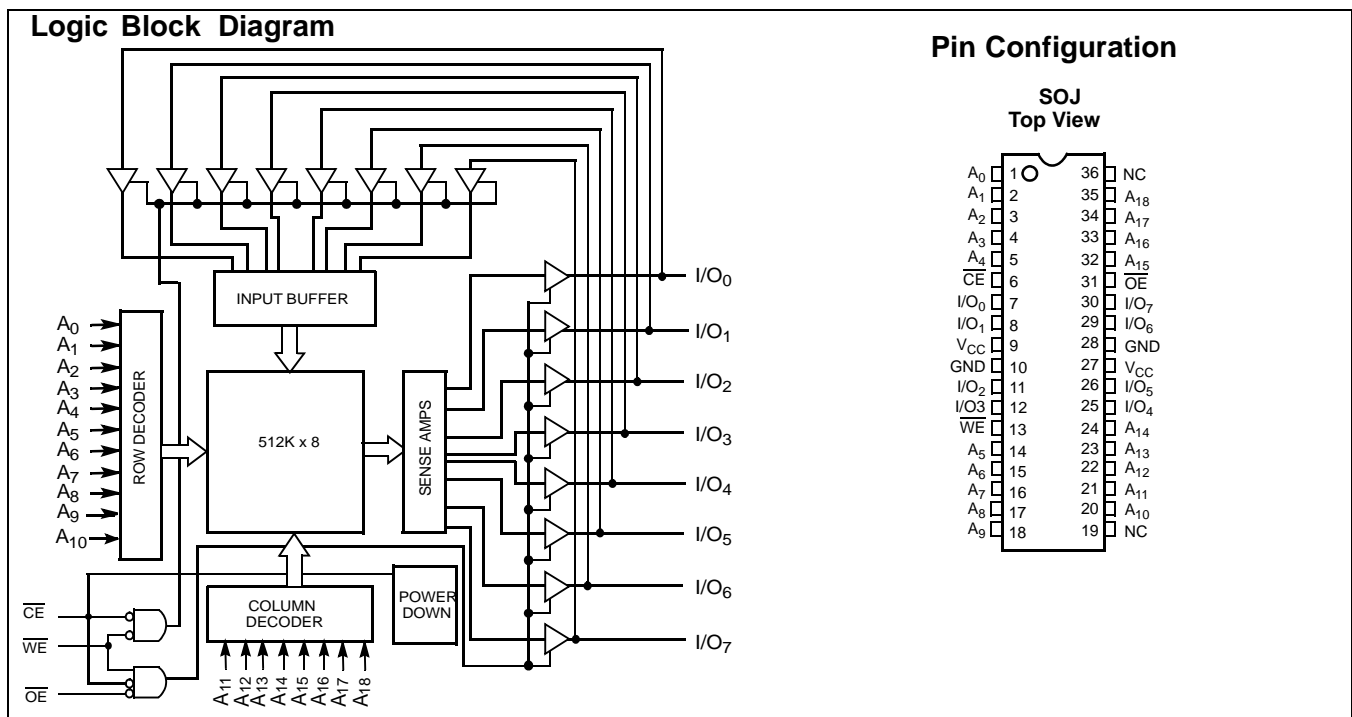## Functional Description[1]

The CY7C1049D is a high-performance CMOS static RAM organized as 512K words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable ($\overline{CE}$), an active LOW Output Enable ($\overline{OE}$), and tri-state drivers. Writing to the device is accomplished by taking Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. Data on the eight I/O pins (I/O$_0$ through I/O$_7$) is then written into the location specified on the address pins (A_0 through A_{18}).

Reading from the device is accomplished by taking Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing Write Enable ($\overline{WE}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins (I/O$_0$ through I/O$_7$) are placed in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}$ LOW, and $\overline{WE}$ LOW).

The CY7C1049D is available in a standard 400-mil-wide 36-pin SOJ package with center power and ground (revolutionary) pinout.

Logic Block Diagram

Pin Configuration

SOJ
Top View

A$_0$	1	36	NC
A$_1$	2	35	A$_{18}$
A$_2$	3	34	A$_{17}$
A$_3$	4	33	A$_{16}$
A$_4$	5	32	A$_{15}$
$\overline{CE}$	6	31	$\overline{OE}$
I/O$_0$	7	30	I/O$_7$
I/O$_1$	8	29	I/O$_6$
V$_{CC}$	9	28	GND
GND	10	27	V$_{CC}$
I/O$_2$	11	26	I/O$_5$
I/O3	12	25	I/O$_4$
$\overline{WE}$	13	24	A$_{14}$
A$_5$	14	23	A$_{13}$
A$_6$	15	22	A$_{12}$
A$_7$	16	21	A$_{11}$
A$_8$	17	20	A$_{10}$
A$_9$	18	19	NC

Selection Guide

	-10	Unit
Maximum Access Time	10	ns
Maximum Operating Current	90	mA
Maximum CMOS Standby Current	10	mA

Note:
1. For guidelines on SRAM system design, please refer to the 'System Design Guidelines' Cypress application note, available on the internet at www.cypress.com.

[+] Feedback

Maximum Ratings

(Above which the useful life may be impaired. For user guide-lines, not tested.)

Storage Temperature ....−65°C to +150°C

Ambient Temperature with
Power Applied..−55°C to +125°C

Supply Voltage on V_{CC} to Relative GND[2] .... −0.5V to +6.0V

DC Voltage Applied to Outputs
in High Z State[2] ....−0.5V to V_{CC} + 0.5V

DC Input Voltage[2] ....−0.5V to V_{CC} + 0.5V

Current into Outputs (LOW).. 20 mA

Static Discharge Voltage..>2001V
(per MIL-STD-883, Method 3015)

Latch-Up Current ....>200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Industrial	−40°C to +85°C	4.5V–5.5V

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		-10 Min.	-10 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4	V
V_{IH}[2]	Input HIGH Voltage			2.0	V_{CC}+ 0.5	V
V_{IL}[2]	Input LOW Voltage[2]			−0.5	0.8	V
I_{IX}	Input Leakage Current	GND < V_I < V_{CC}		−1	+1	µA
I_{OZ}	Output Leakage Current	GND < V_{OUT} < V_{CC}, Output Disabled		−1	+1	µA
I_{CC}	VCC Operating Supply Current	V_{CC} = Max., f = f_{MAX} = 1/t_{RC}	100 MHz		90	mA
			83 MHz		80	mA
			66 MHz		70	mA
			40 MHz		60	mA
I_{SB1}	Automatic CE Power-Down Current —TTL Inputs	Max. V_{CC}, CE > V_{IH}, V_{IN} > V_{IH} or V_{IN} < V_{IL}, f = f_{MAX}			20	mA
I_{SB2}	Automatic CE Power-Down Current —CMOS Inputs	Max. V_{CC}, CE > V_{CC} − 0.3V, V_{IN} > V_{CC} − 0.3V, or V_{IN} < 0.3V, f = 0			10	mA

Capacitance[3]

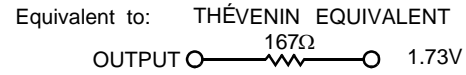| Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	8	pF
C_{OUT}	I/O Capacitance		8	pF

Thermal Resistance[3]

Parameter	Description	Test Conditions	SOJ Package	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)[3]	Still Air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	57.91	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)[3]		36.73	°C/W

Notes:
2. Minimum voltage is −2.0V and V_{IH}(max) = V_{CC} + 2V for pulse durations of less than 20 ns.
3. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms[4]
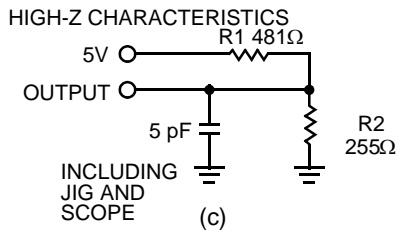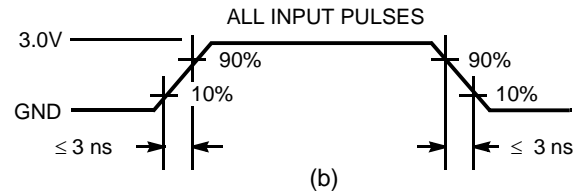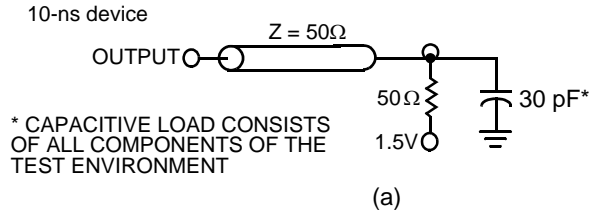
10-ns device

(a)

* CAPACITIVE LOAD CONSISTS OF ALL COMPONENTS OF THE TEST ENVIRONMENT

HIGH-Z CHARACTERISTICS

(c)

INCLUDING JIG AND SCOPE

ALL INPUT PULSES

(b)

Equivalent to: THÉVENIN EQUIVALENT

167Ω

OUTPUT ——WW—— 1.73V

Switching Characteristics[5] Over the Operating Range

Parameter	Description	-10		Unit
		Min.	Max.	
Read Cycle				
t_{power}	V_{CC}(typical) to the First Access[6]	100		μs
t_{RC}	Read Cycle Time	10		ns
t_{AA}	Address to Data Valid		10	ns
t_{OHA}	Data Hold from Address Change	3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		10	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		5	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[8]	0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[7, 8]		5	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[8]	3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[7, 8]		5	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		10	ns
Write Cycle[9, 10]				
t_{WC}	Write Cycle Time	10		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	7		ns
t_{AW}	Address Set-Up to Write End	7		ns
t_{HA}	Address Hold from Write End	0		ns

Notes:
4. AC characteristics (except High-Z) for 10-ns parts are tested using the load conditions shown in Figure (a). High-Z characteristics are tested for all speeds using the test load shown in Figure (c)
5. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
6. t_{POWER} gives the minimum amount of time that the power supply should be at typical V_{CC} values until the first memory access can be performed.
7. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (c) of AC Test Loads. Transition is measured when the outputs enter a high impedance state.
8. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
9. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW, and $\overline{WE}$ LOW. $\overline{CE}$ and $\overline{WE}$ must be LOW to initiate a write, and the transition of either of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
10. The minimum write cycle time for Write Cycle no. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

Switching Characteristics[5] Over the Operating Range (continued)

Parameter	Description	-10		Unit
		Min.	**Max.**	
t_{SA}	Address Set-Up to Write Start	0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	7		ns
t_{SD}	Data Set-Up to Write End	6		ns
t_{HD}	Data Hold from Write End	0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[8]	3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[7, 8]		5	ns

Data Retention Characteristics Over the Operating Range

Parameter	Description	Conditions[12]	Min.	Max	Unit
V_{DR}	V_{CC} for Data Retention		2.0		V
I_{CCDR}	Data Retention Current	$V_{CC} = V_{DR} = 2.0V$, $\overline{CE} \geq V_{CC} - 0.3V$ $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$		10	mA
t_{CDR}[3]	Chip Deselect to Data Retention Time		0		ns
t_R[11]	Operation Recovery Time		t_{RC}		ns

Data Retention Waveform
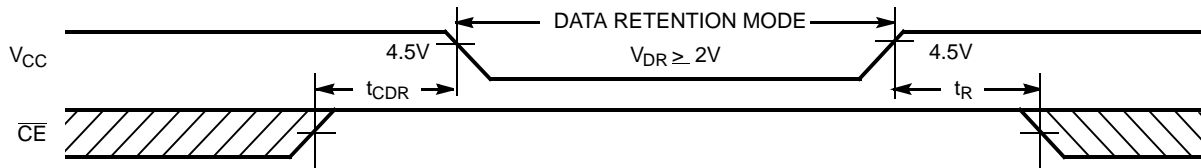
Switching Waveforms

Read Cycle No. 1[13, 14]
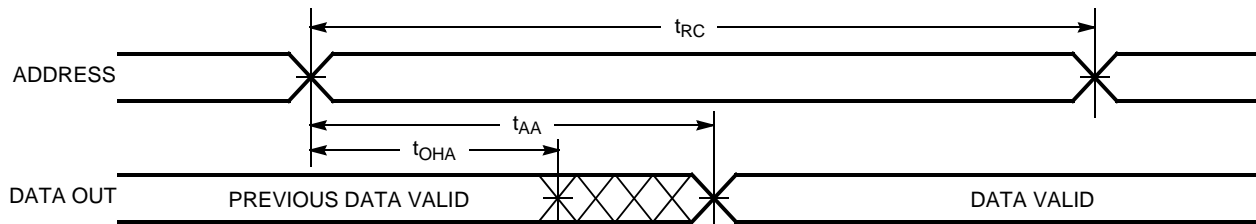
Notes:
11. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min.)} \geq 50 \mu s$ or stable at $V_{CC(min.)} \geq 50 \mu s$
12. No input may exceed V_{CC} + 0.5V.
13. Device is continuously selected. $\overline{OE}$, $\overline{CE} = V_{IL}$.
14. $\overline{WE}$ is HIGH for read cycle.

[+] Feedback

Switching Waveforms(continued)

Read Cycle No. 2 ($\overline{OE}$ Controlled)[14, 15]
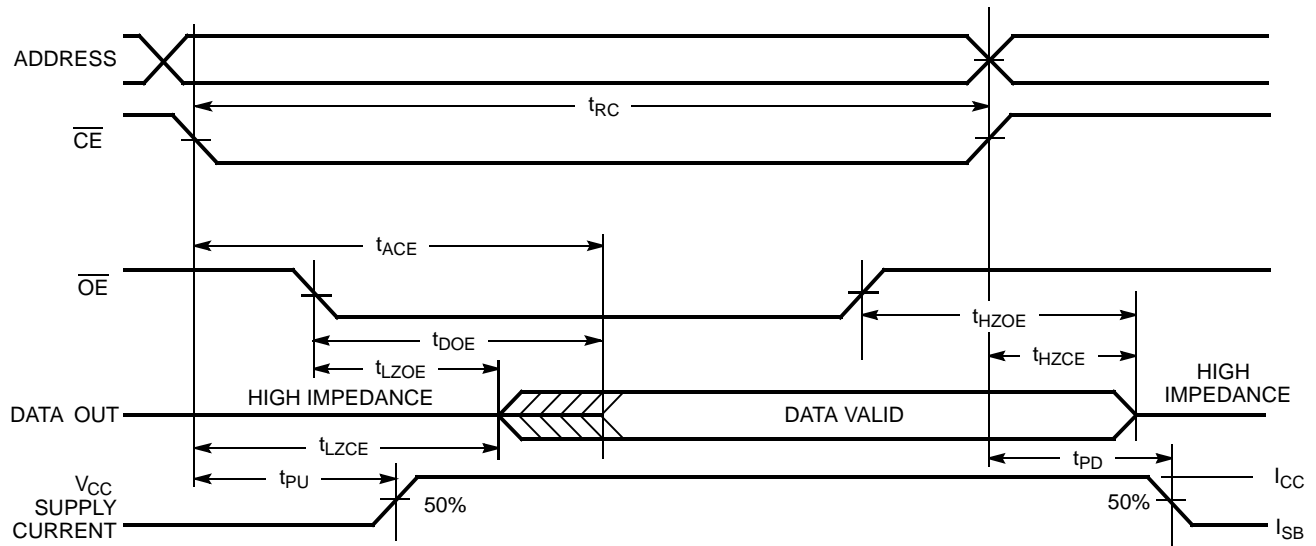
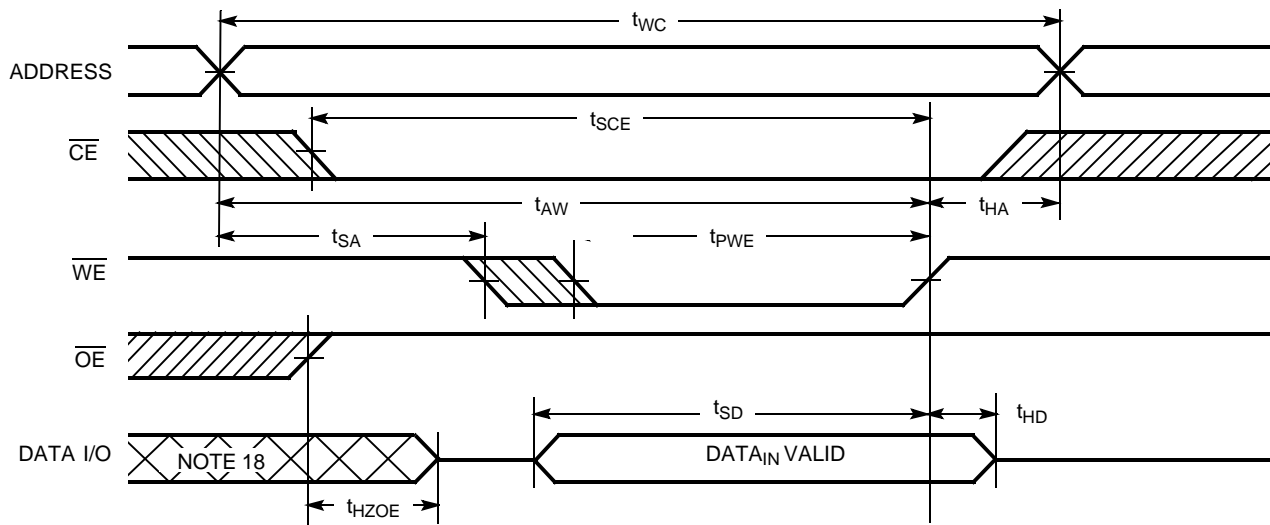
**Write Cycle No. 1 ($\overline{CE}$ Controlled)**[16, 17]
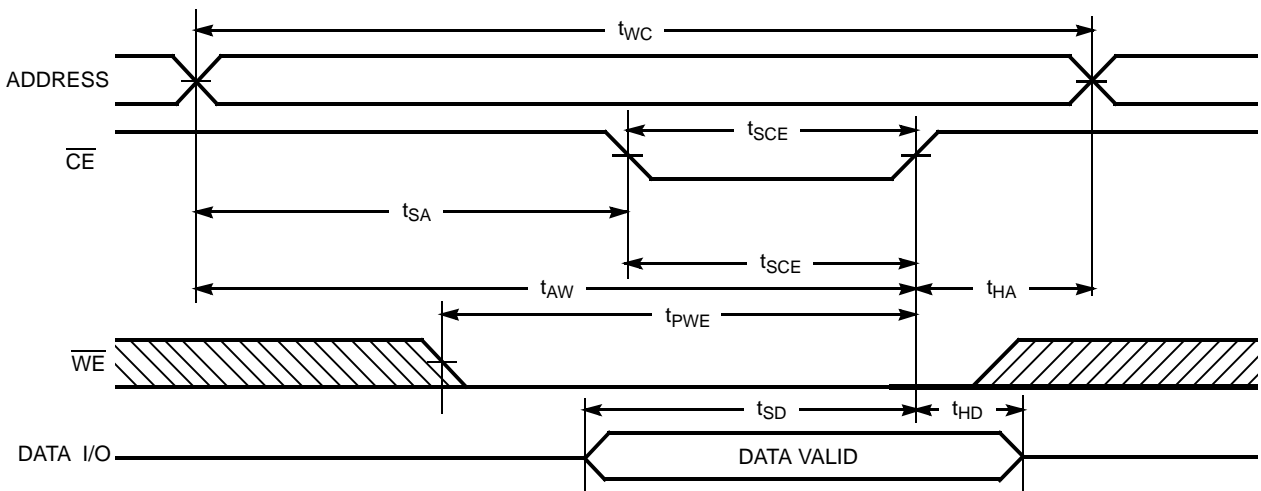
Notes:
15. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
16. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
17. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.

Switching Waveforms(continued)

Write Cycle No. 2 (WE Controlled, OE HIGH During Write)[16, 17]

Write Cycle No. 3 (WE Controlled, OE LOW)[17]
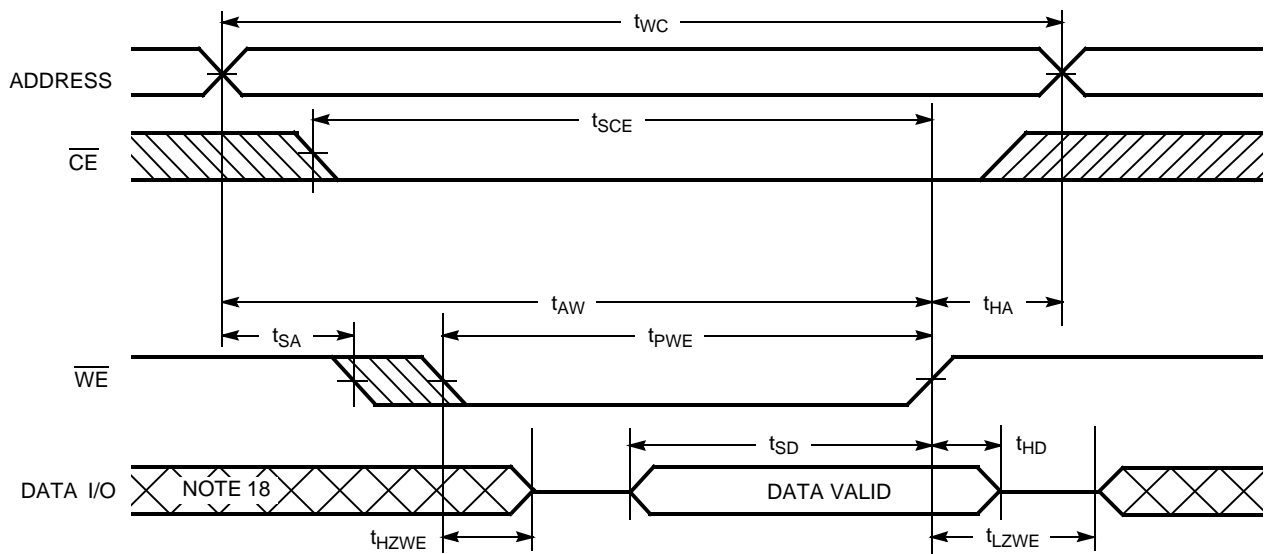
Truth Table

CE	OE	WE	I/O$_0$–I/O$_7$	Mode	Power
H	X	X	High-Z	Power-down	Standby (I$_{SB}$)
L	L	H	Data Out	Read	Active (I$_{CC}$)
L	X	L	Data In	Write	Active (I$_{CC}$)
L	H	H	High-Z	Selected, Outputs Disabled	Active (I$_{CC}$)

Notes:
18. During this period the I/Os are in the output state and input signals should not be applied.

[+] Feedback

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C1049D-10VXI	51-85090	36-Lead (400-Mil) Molded SOJ (Pb-Free)	Industrial

Please contact your local Cypress sales representative for availability of these parts.

Package Diagram

36-Lead (400-Mil) Molded SOJ (51-85090)

DIMENSIONS IN INCHES MIN.
MAX.

DIM. A	
ANAM	CSPI
.086 .090	.095 .115

51-85090-*B
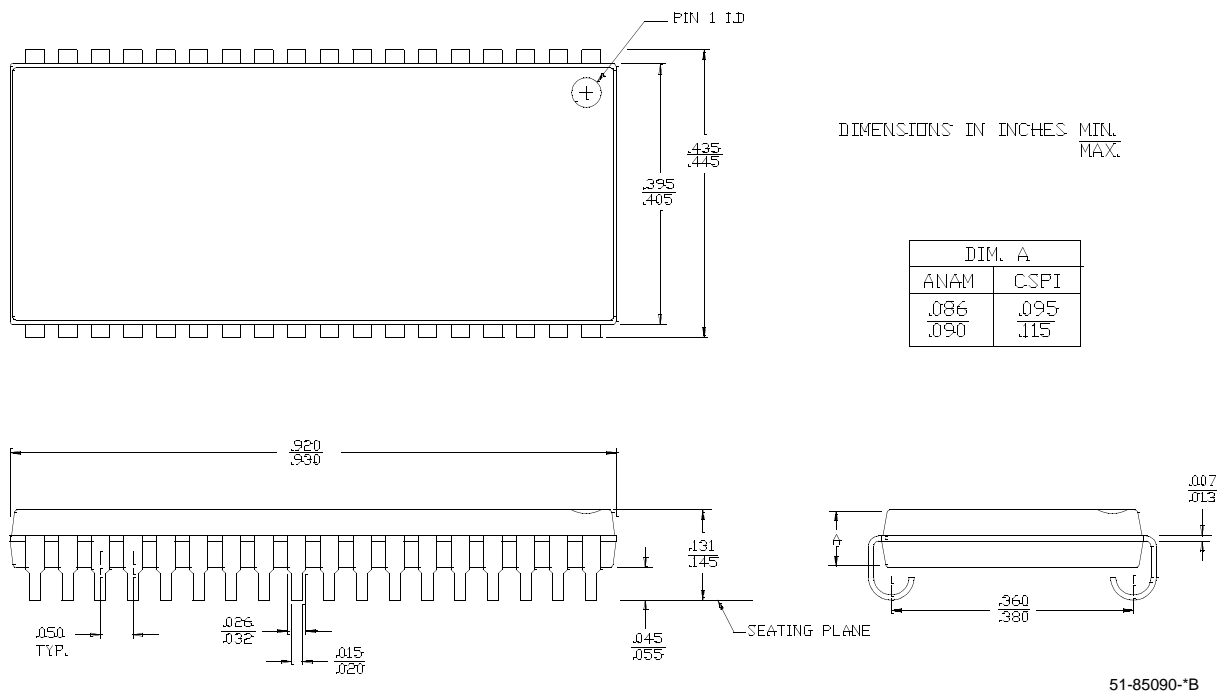
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Document History Page

Document Title: CY7C1049D 4-Mbit (512K x 8) Static RAM
Document Number: 38-05474

REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	201560	See ECN	SWI	Advance Datasheet for C9 IPP
*A	233729	See ECN	RKF	1.AC, DC parameters are modified as per EROS(Spec # 01-2165) 2.Pb-free offering in the 'ordering information'
*B	351096	See ECN	PCI	Changed from Advance to Preliminary Removed 17, 20 ns Speed bin Added footnote # 4 Redefined I_{CC} values for Com'l and Ind'l temperature ranges I_{CC} (Com'l): Changed from 67 and 54 mA to 75 and 70 mA for 12 and 15 ns speed bins respectively I_{CC} (Ind'l): Changed from 80, 67 and 54 mA to 90, 85 and 80 mA for 10, 12 and 15 ns speed bins respectively Added $V_{IH(max)}$ spec in Note# 2 Modified Note# 10 on t_R Changed t_{SCE} from 8 to 7 ns for 10 ns speed bin Changed reference voltage level for measurement of Hi-Z parameters from ±500 mV to ±200 mV Added Truth Table on page# 6 Removed L-Version Added 10 ns parts in the Ordering Information Table Added Lead-Free Product Information Shaded Ordering Information Table
*C	446328	See ECN	NXR	Converted from Preliminary to Final Removed -12 and -15 speed bins Removed Commercial Operating Range product information Changed Maximum Rating for supply voltage from 7V to 6V Updated Thermal Resistance table Changed t_{HZWE} from 6 ns to 5 ns Updated footnote #7 on High-Z parameter measurement Replaced Package Name column with Package Diagram in the Ordering Information table

[+] Feedback