

4-Mbit (1M x 4) Static RAM

Features

- Pin- and function-compatible with CY7C1046CV33
- High speed
 - $t_{AA} = 10 \text{ ns}$
- Low active power
 - $I_{CC} = 90 \text{ mA @ } 10 \text{ ns}$
- Low CMOS standby power
 - $I_{SB2} = 10 \text{ mA}$
- 2.0 V data retention
- Automatic power-down when deselected
- TTL-compatible inputs and outputs
- Easy memory expansion with \overline{CE} and \overline{OE} features
- Available in lead-free 400-mil-wide 32-pin SOJ package

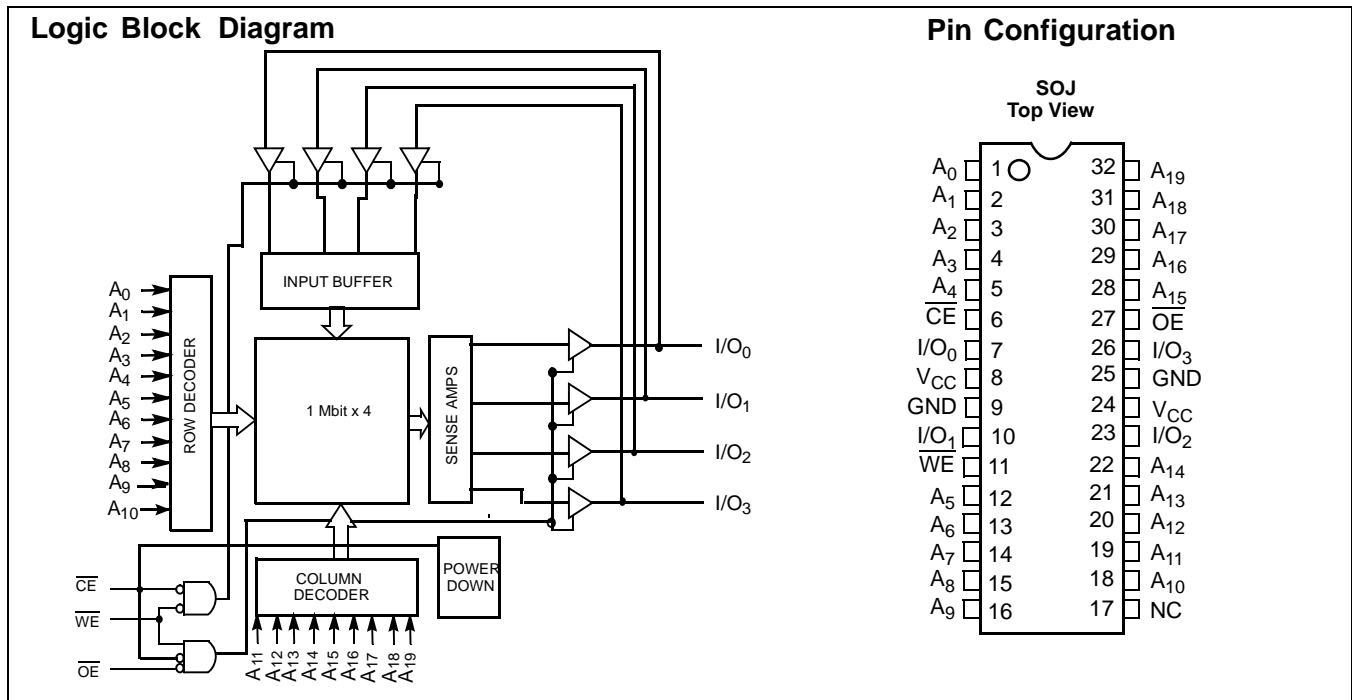
Functional Description^[1]

The CY7C1046DV33 is a high-performance CMOS static RAM organized as 1M words by 4 bits. Easy memory expansion is provided by an active LOW Chip Enable (\overline{CE}), an active LOW Output Enable (\overline{OE}), and tri-state drivers. Writing to the device is accomplished by taking Chip Enable (\overline{CE}) and Write Enable (\overline{WE}) inputs LOW. Data on the four I/O pins (I/O_0 through I/O_3) is then written into the location specified on the address pins (A_0 through A_{19}).

Reading from the device is accomplished by taking Chip Enable (\overline{CE}) and Output Enable (\overline{OE}) LOW while forcing Write Enable (\overline{WE}) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The four input/output pins (I/O_0 through I/O_3) are placed in a high-impedance state when the device is deselected (\overline{CE} HIGH), the outputs are disabled (\overline{OE} HIGH), or during a Write operation (\overline{CE} LOW, and \overline{WE} LOW).

The CY7C1046DV33 is available in a standard 400-mil-wide 32-pin SOJ package with center power and ground (revolutionary) pinout.



Selection Guide

	-10	Unit
Maximum Access Time	10	ns
Maximum Operating Current	90	mA
Maximum CMOS Standby Current	10	mA

Note:

1. For guidelines on SRAM system design, please refer to the *System Design Guidelines* Cypress application note, available on the internet at www.cypress.com.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C
 Ambient Temperature with Power Applied..... -55°C to +125°C
 Supply Voltage on V_{CC} to Relative GND^[2] -0.3 to +4.6V
 DC Voltage Applied to Outputs in High-Z State^[2] -0.3V to V_{CC} +0.3V

DC Input Voltage^[2] -0.3V to V_{CC} +0.3V
 Current into Outputs (LOW)..... 20 mA
 Static Discharge Voltage..... > 2001V (per MIL-STD-883, Method 3015)
 Latch-up Current..... > 200 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Industrial	-40°C to +85°C	3.3V ± 0.3V

DC Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	-10		Unit
			Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4.0 mA	2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4	V
V _{IH}	Input HIGH Voltage		2.0	V _{CC} + 0.3	V
V _{IL}	Input LOW Voltage ^[2]		-0.3	0.8	V
I _{IX}	Input Leakage Current	GND ≤ V _I ≤ V _{CC}	-1	+1	μA
I _{OZ}	Output Leakage Current	GND ≤ V _{OUT} ≤ V _{CC} , Output Disabled	-1	+1	μA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., f = f _{MAX} = 1/t _{RC}	100 MHz	90	mA
			83 MHz	80	
			66 MHz	70	mA
			40 MHz	60	
I _{SB1}	Automatic CE Power-Down Current —TTL Inputs	Max. V _{CC} , $\overline{CE} \geq V_{IH}$, V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{MAX}		20	mA
I _{SB2}	Automatic CE Power-Down Current —CMOS Inputs	Max. V _{CC} , $\overline{CE} \geq V_{CC} - 0.3V$, V _{IN} ≥ V _{CC} - 0.3V, or V _{IN} ≤ 0.3V, f = 0		10	mA

Capacitance^[3]

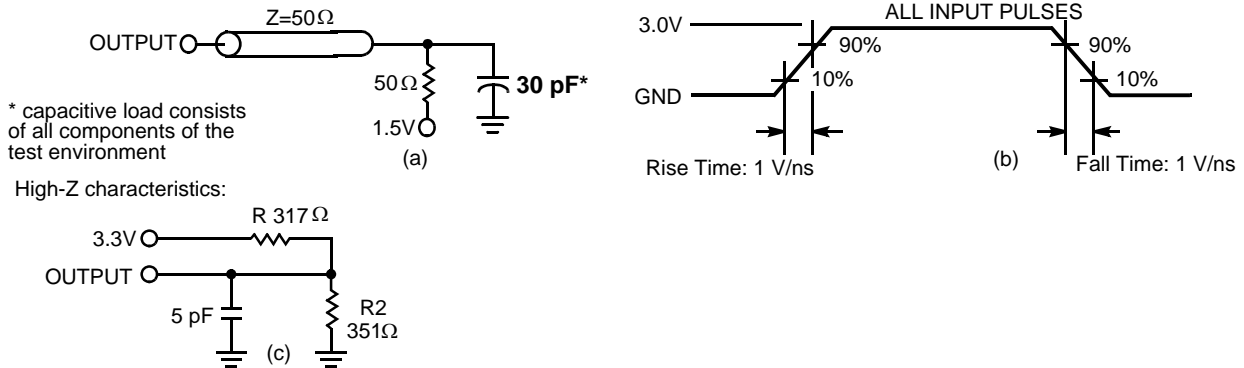
Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 3.3V	8	pF
C _{OUT}	I/O Capacitance		8	pF

Thermal Resistance^[3]

Parameter	Description	Test Conditions	SOJ Package	Unit
Θ _{JA}	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	53.44	°C/W
Θ _{JC}	Thermal Resistance (Junction to Case)		38.25	°C/W

Notes:

- V_{IL} (min.) = -2.0V and V_{IH} (max) = V_{CC} +2V for pulse durations of less than 20 ns.
- Tested initially and after any design or process changes that may affect these parameters

AC Test Loads and Waveforms^[4]

AC Switching Characteristics Over the Operating Range^[5]

Parameter	Description	-10		Unit
		Min.	Max.	
Read Cycle				
$t_{power}^{[6]}$	V_{CC} (typical) to the first access	100		μs
t_{RC}	Read Cycle Time	10		ns
t_{AA}	Address to Data Valid		10	ns
t_{OHA}	Data Hold from Address Change	3		ns
t_{ACE}	\overline{CE} LOW to Data Valid		10	ns
t_{DOE}	\overline{OE} LOW to Data Valid		5	ns
t_{LZOE}	\overline{OE} LOW to Low-Z ^[8]	0		ns
t_{HZOE}	\overline{OE} HIGH to High-Z ^[7, 8]		5	ns
t_{LZCE}	\overline{CE} LOW to Low-Z ^[8]	3		ns
t_{HZCE}	\overline{CE} HIGH to High-Z ^[7, 8]		5	ns
t_{PU}	\overline{CE} LOW to Power-up	0		ns
t_{PD}	\overline{CE} HIGH to Power-Down		10	ns
Write Cycle^[9, 10]				
t_{WC}	Write Cycle Time	10		ns
t_{SCE}	\overline{CE} LOW to Write End	7		ns
t_{AW}	Address Set-up to Write End	7		ns
t_{HA}	Address Hold from Write End	0		ns
t_{SA}	Address Set-up to Write Start	0		ns
t_{PWE}	\overline{WE} Pulse Width	7		ns
t_{SD}	Data Set-up to Write End	5		ns
t_{HD}	Data Hold from Write End	0		ns
t_{LZWE}	\overline{WE} HIGH to Low-Z ^[8]	3		ns
t_{HZWE}	\overline{WE} LOW to High-Z ^[7, 8]		5	ns

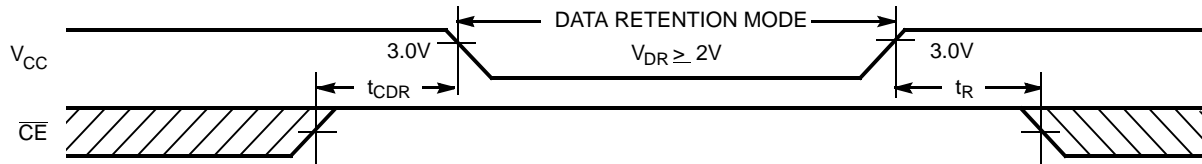
Notes:

- AC characteristics (except High-Z) are tested using the load conditions shown in (a). High-Z characteristics are tested for all speeds using the test load shown in (c).
- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V.
- t_{power} gives the minimum amount of time that the power supply should be at stable, typical V_{CC} values until the first memory access can be performed.
- t_{HZOE} , t_{HZCE} , and t_{HZWE} are specified with a load capacitance of 5 pF as in part (c) of AC Test Loads. Transition is measured when the outputs enter a high impedance state.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
- The internal Write time of the memory is defined by the overlap of \overline{CE} LOW, and \overline{WE} LOW. \overline{CE} and \overline{WE} must be LOW to initiate a Write, and the transition of either of these signals can terminate the Write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the Write.
- The minimum Write cycle time for Write Cycle no. 3 (\overline{WE} controlled, \overline{OE} LOW) is the sum of t_{HZWE} and t_{SD} .

Data Retention Characteristics Over the Operating Range

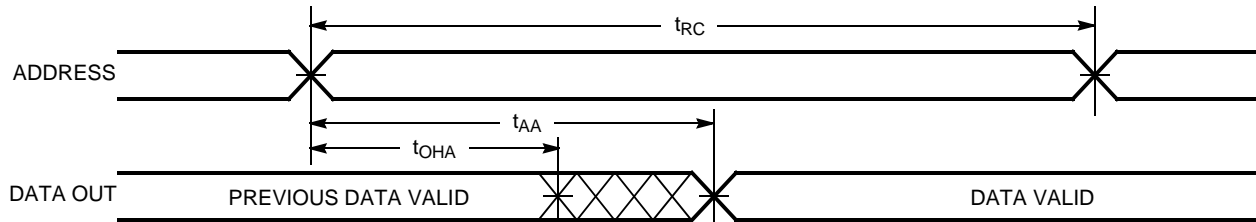
Parameter	Description	Conditions ^[11]	Min.	Max	Unit
V_{DR}	V_{CC} for Data Retention		2.0		V
I_{CCDR}	Data Retention Current	$V_{CC} = V_{DR} = 2.0V$, $CE \geq V_{CC} - 0.3V$		10	mA
$t_{CDR}^{[3]}$	Chip Deselect to Data Retention Time	$V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$	0		ns
$t_R^{[12]}$	Operation Recovery Time		t_{RC}		ns

Data Retention Waveform

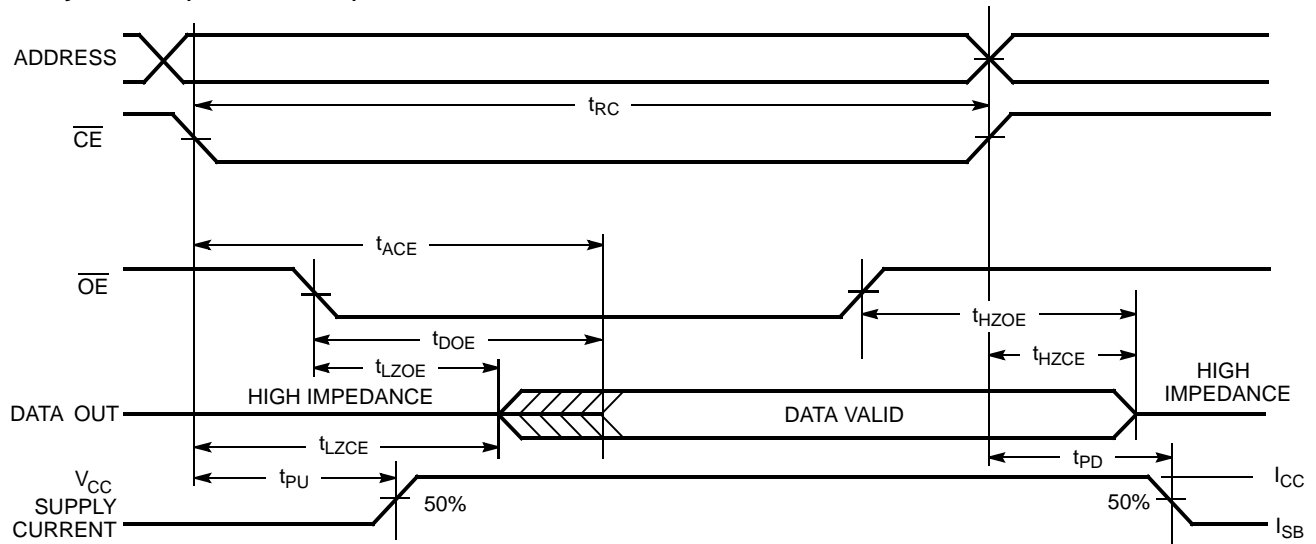


Switching Waveforms

Read Cycle No. 1^[13, 14]



Read Cycle No. 2 (\overline{OE} Controlled)^[14, 15]

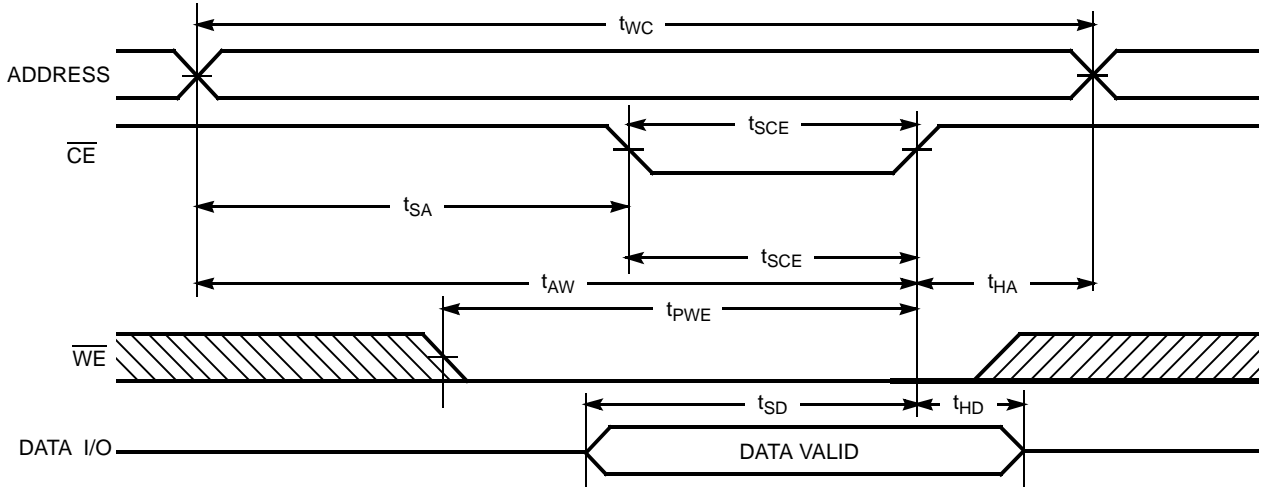


Notes:

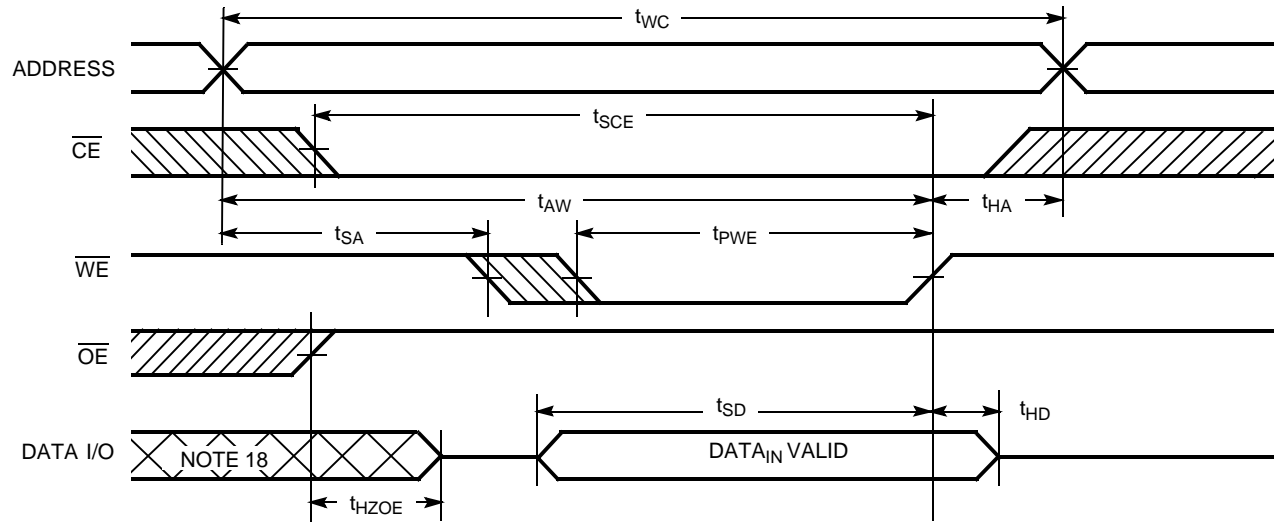
11. No inputs may exceed $V_{CC} + 0.3V$
12. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min.)} \geq 50 \mu s$ or stable at $V_{CC(min.)} \geq 50 \mu s$
13. Device is continuously selected. $\overline{OE}, CE = V_{IL}$.
14. \overline{WE} is HIGH for Read cycle.
15. Address valid prior to or coincident with \overline{CE} transition LOW.

Switching Waveforms (continued)

Write Cycle No. 1 (\overline{CE} Controlled)^[16, 17]



Write Cycle No. 2 (\overline{WE} Controlled, \overline{OE} HIGH During Write)^[16, 17]

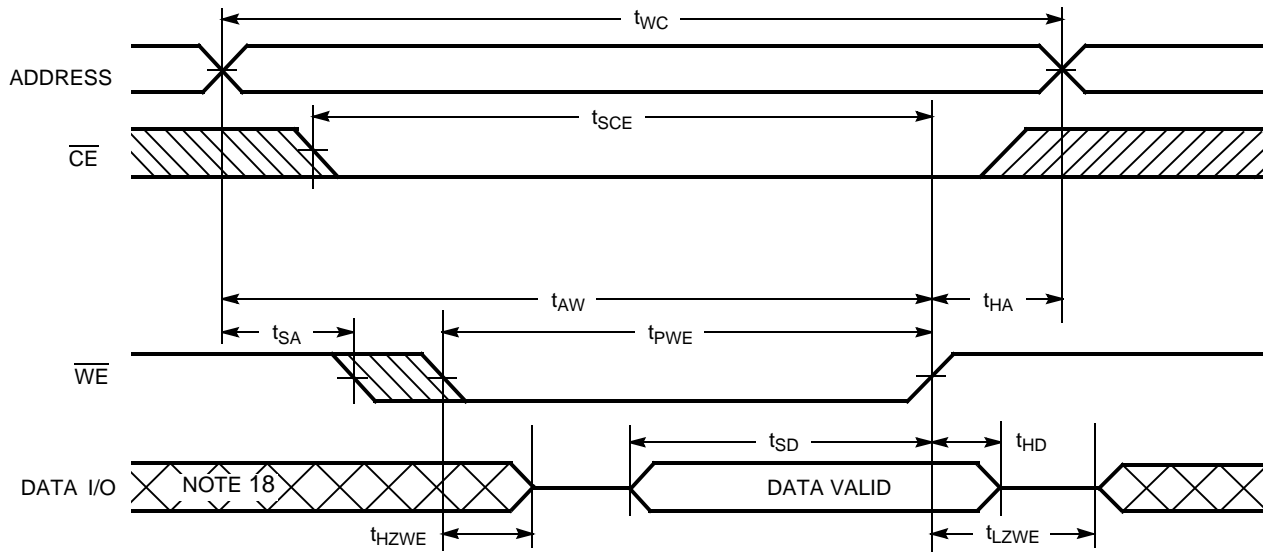


Notes:

- 16. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
- 17. If \overline{CE} goes HIGH simultaneously with \overline{WE} going HIGH, the output remains in a high-impedance state.
- 18. During this period the I/Os are in the output state and input signals should not be applied.

Switching Waveforms (continued)

Write Cycle No. 3 (\overline{WE} Controlled, \overline{OE} LOW)^[17]



Truth Table

\overline{CE}	\overline{OE}	\overline{WE}	I/O ₀ - I/O ₃	Mode	Power
H	X	X	High-Z	Power-down	Standby (I_{SB})
L	L	H	Data Out	Read	Active (I_{CC})
L	X	L	Data In	Write	Active (I_{CC})
L	H	H	High-Z	Selected, Outputs Disabled	Active (I_{CC})

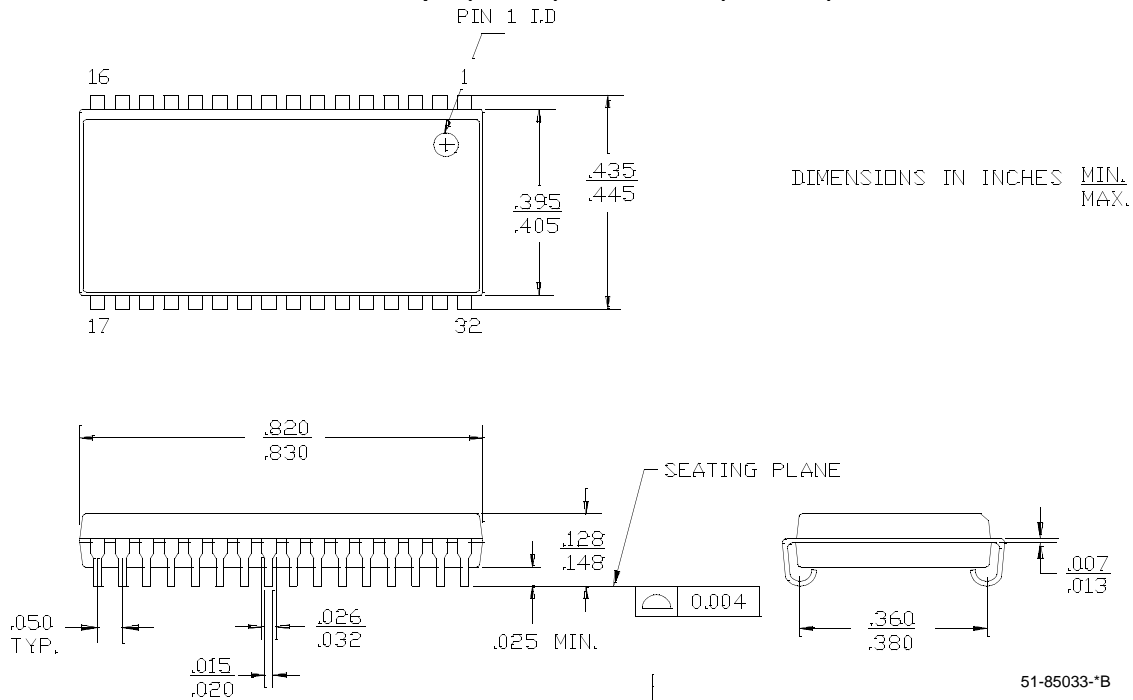
Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C1046DV33-10VXI	51-85033	32-lead (400-mil) Molded SOJ (Pb-Free)	Industrial

Please contact your local Cypress sales representative for availability of these parts.

Package Diagram

32-pin (400-Mil) Molded SOJ (51-85033)



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Document History Page

Document Title: CY7C1046DV33 4-Mbit (1M x4) Static RAM				
Document Number: 38-05611				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	307613	See ECN	RKF	New data sheet
*A	397134	See ECN	R XU	<p>Changed from Advance to Preliminary</p> <p>Changed address of Cypress Semiconductor Corporation on Page# 1 from "3901 North First Street" to "198 Champion Court"</p> <p>Removed -15 Speed bin</p> <p>Corrected DC voltage limits in maximum ratings section from - 0.5 to - 0.3V and $V_{CC} + 0.5V$ to $V_{CC} + 0.3V$</p> <p>Redefined I_{CC} values for Com'l and Ind'l temperature ranges</p> <p>I_{CC} (Com'l): Changed from 100, 80 and 70 mA to 90, 80 and 75 mA for 8, 10 and 12ns speed bins respectively</p> <p>I_{CC} (Ind'l): Changed from 80 and 70 mA to 90 and 85 mA for 10 and 12ns speed bins respectively</p> <p>Removed footnote on rise time and added footnote on Operation Recovery Time (t_R)</p> <p>Corrected Typo in Truth Table from (I/O₀ - I/O₇) to (I/O₀ to I/O₃)</p> <p>Changed part names from V33 to V32 in the Ordering Information Table</p> <p>Removed L-Version</p> <p>Added Lead-Free Product Information</p> <p>Shaded Ordering Information Table</p>
*B	459072	See ECN	NXR	<p>Converted from Preliminary to Final</p> <p>Removed -8 and -12 speed bins</p> <p>Removed Commercial Operating Range product information</p> <p>Removed the PIn Definition table</p> <p>Changed the Capacitance value of input pins and I/O pins from 6 pF to 8 pF</p> <p>Updated the Thermal Resistance table</p> <p>Updated footnote #7 on High-Z parameter measurement</p> <p>Added footnote #11</p> <p>Replaced Package Name column with Package Diagram in the Ordering Information table</p>