

# 1-Mbit (128K x 8) Static RAM

## Features

- Pin- and function-compatible with CY7C1019B
- High speed
  - $t_{AA} = 10 \text{ ns}$
- Low active power
  - $I_{CC} = 80 \text{ mA @ } 10 \text{ ns}$
- Low CMOS standby power
  - $I_{SB2} = 3 \text{ mA}$
- 2.0V Data retention
- Automatic power-down when deselected
- CMOS for optimum speed/power
- Center power/ground pinout
- Easy memory expansion with  $\overline{CE}$  and  $\overline{OE}$  options
- Functionally equivalent to CY7C1019B
- Available in Pb-free 32-pin 400-Mil wide Molded SOJ and 32-pin TSOP II packages

## Functional Description <sup>[1]</sup>

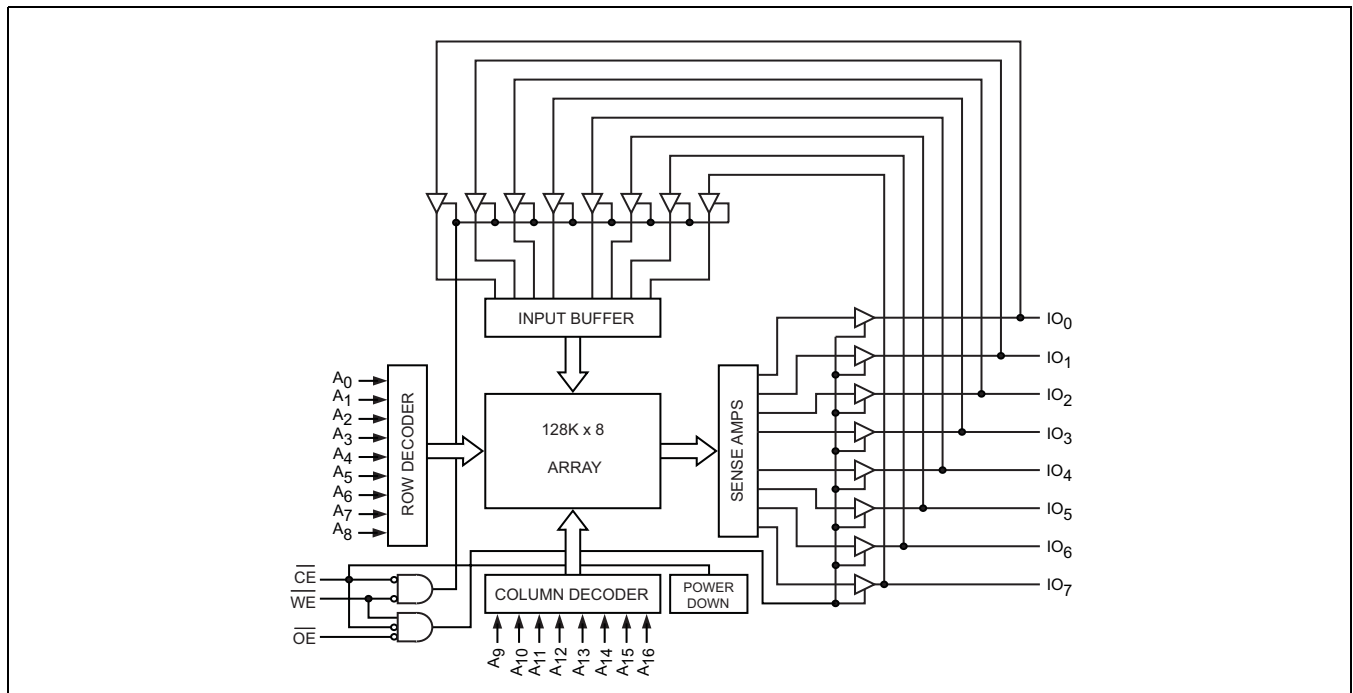
The CY7C1019D is a high-performance CMOS static RAM organized as 131,072 words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable ( $\overline{CE}$ ), an active LOW Output Enable ( $\overline{OE}$ ), and tri-state drivers. This device has an automatic power-down feature that significantly reduces power consumption when deselected. The eight input and output pins ( $IO_0$  through  $IO_7$ ) are placed in a high-impedance state when:

- Deselected ( $\overline{CE}$  HIGH)
- Outputs are disabled ( $\overline{OE}$  HIGH)
- When the write operation is active ( $\overline{CE}$  LOW, and  $\overline{WE}$  LOW).

Write to the device by taking Chip Enable ( $\overline{CE}$ ) and Write Enable ( $\overline{WE}$ ) inputs LOW. Data on the eight IO pins ( $IO_0$  through  $IO_7$ ) is then written into the location specified on the address pins ( $A_0$  through  $A_{16}$ ).

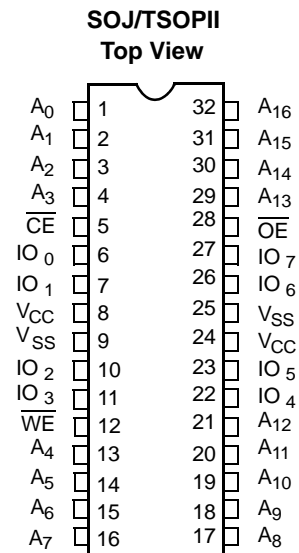
Read from the device by taking Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) LOW while forcing Write Enable ( $\overline{WE}$ ) HIGH. Under these conditions, the contents of the memory location specified by the address pins appears on the IO pins.

## Logic Block Diagram



### Note

1. For guidelines on SRAM system design, please refer to the 'System Design Guidelines' Cypress application note, available on the internet at [www.cypress.com](http://www.cypress.com).

**Pin Configuration**

**Selection Guide**

|                           | <b>-10 (Industrial)</b> | <b>Unit</b> |
|---------------------------|-------------------------|-------------|
| Maximum Access Time       | 10                      | ns          |
| Maximum Operating Current | 80                      | mA          |
| Maximum Standby Current   | 3                       | mA          |

### Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with Power Applied..... -55°C to +125°C  
Supply Voltage on V<sub>CC</sub> to Relative GND [2] ... -0.5V to +6.0V

DC Voltage Applied to Outputs in High-Z State [2] ..... -0.5V to V<sub>CC</sub> + 0.5V

DC Input Voltage [2] ..... -0.5V to V<sub>CC</sub> + 0.5V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage..... > 2001V (per MIL-STD-883, Method 3015)

Latch-up Current ..... > 200 mA

### Operating Range

| Range      | Ambient Temperature | V <sub>CC</sub> | Speed |
|------------|---------------------|-----------------|-------|
| Industrial | -40°C to +85°C      | 5V ± 0.5V       | 10 ns |

### Electrical Characteristics (Over the Operating Range)

| Parameter        | Description                                 | Test Conditions  | -10 (Industrial) |                       | Unit |
|------------------|---|--|------------------|-----------------------|------|
|                  |   |  | Min              | Max                   |      |
| V <sub>OH</sub>  | Output HIGH Voltage                         | I <sub>OH</sub> = -4.0 mA  | 2.4              |                       | V    |
| V <sub>OL</sub>  | Output LOW Voltage                          | I <sub>OL</sub> = 8.0 mA   |                  | 0.4                   | V    |
| V <sub>IH</sub>  | Input HIGH Voltage                          |  | 2.2              | V <sub>CC</sub> + 0.5 | V    |
| V <sub>IL</sub>  | Input LOW Voltage [2]                       |  | -0.5             | 0.8                   | V    |
| I <sub>IX</sub>  | Input Leakage Current                       | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>   | -1               | +1                    | μA   |
| I <sub>OZ</sub>  | Output Leakage Current                      | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub> , Output Disabled   | -1               | +1                    | μA   |
| I <sub>CC</sub>  | V <sub>CC</sub> Operating Supply Current    | V <sub>CC</sub> = Max,<br>I <sub>OUT</sub> = 0 mA,<br>f = f <sub>max</sub> = 1/t <sub>RC</sub>   | 100 MHz          | 80                    | mA   |
|                  |   |  | 83 MHz           | 72                    | mA   |
|                  |   |  | 66 MHz           | 58                    | mA   |
|                  |   |  | 40 MHz           | 37                    | mA   |
| I <sub>SB1</sub> | Automatic CE Power-Down Current—TTL Inputs  | Max V <sub>CC</sub> , $\overline{CE} \geq V_{IH}$<br>V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>max</sub> |                  | 10                    | mA   |
| I <sub>SB2</sub> | Automatic CE Power-Down Current—CMOS Inputs | Max V <sub>CC</sub> , $\overline{CE} \geq V_{CC} - 0.3V$ ,<br>V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V, or V <sub>IN</sub> ≤ 0.3V, f = 0           |                  | 3                     | mA   |

**Note**

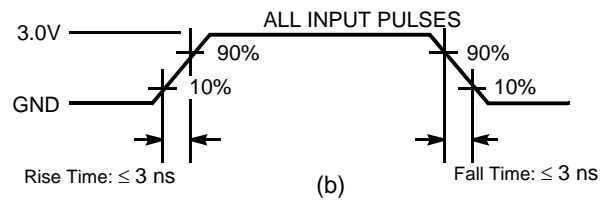
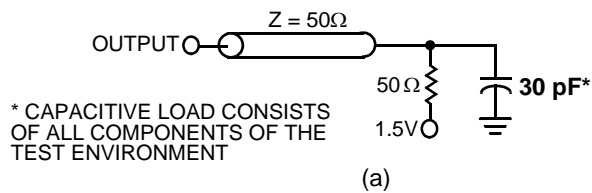
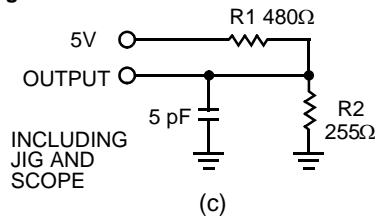
2. V<sub>IL</sub>(min) = -2.0V and V<sub>IH</sub>(max) = V<sub>CC</sub> + 1V for pulse durations of less than 5 ns.

**Capacitance** <sup>[3]</sup>

| Parameter        | Description        | Test Conditions  | Max | Unit |
|------------------|--------------------|--|-----|------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 5.0V | 6   | pF   |
| C <sub>OUT</sub> | Output Capacitance |  | 8   | pF   |

**Thermal Resistance** <sup>[3]</sup>

| Parameter       | Description                              | Test Conditions   | 400-Mil Wide SOJ | TSOP II | Unit |
|-----------------|--|---|------------------|---------|------|
| Θ <sub>JA</sub> | Thermal Resistance (Junction to Ambient) | Still Air, soldered on a 3 × 4.5 inch, four-layer printed circuit board | 56.29            | 62.22   | °C/W |
| Θ <sub>JC</sub> | Thermal Resistance (Junction to Case)    |   | 38.14            | 21.43   | °C/W |

**AC Test Loads and Waveforms** <sup>[4]</sup>

**High-Z characteristics:**

**Notes**

3. Tested initially and after any design or process changes that may affect these parameters.
4. AC characteristics (except High-Z) are tested using the load conditions shown in Figure (a). High-Z characteristics are tested for all speeds using the test load shown in Figure (c).

**Switching Characteristics** (Over the Operating Range) <sup>[5]</sup>

| Parameter                              | Description                                      | -10 (Industrial) |     | Unit    |
|--|--|------------------|-----|---------|
|  |  | Min              | Max |         |
| <b>Read Cycle</b>                      |  |                  |     |         |
| $t_{power}^{[6]}$                      | $V_{CC}$ (typical) to the first access           | 100              |     | $\mu$ S |
| $t_{RC}$                               | Read Cycle Time                                  | 10               |     | ns      |
| $t_{AA}$                               | Address to Data Valid                            |                  | 10  | ns      |
| $t_{OHA}$                              | Data Hold from Address Change                    | 3                |     | ns      |
| $t_{ACE}$                              | $\overline{CE}$ LOW to Data Valid                |                  | 10  | ns      |
| $t_{DOE}$                              | $\overline{OE}$ LOW to Data Valid                |                  | 5   | ns      |
| $t_{LZOE}$                             | $\overline{OE}$ LOW to Low Z                     | 0                |     | ns      |
| $t_{HZOE}$                             | $\overline{OE}$ HIGH to High Z <sup>[7, 8]</sup> |                  | 5   | ns      |
| $t_{LZCE}$                             | $\overline{CE}$ LOW to Low Z <sup>[8]</sup>      | 3                |     | ns      |
| $t_{HZCE}$                             | $\overline{CE}$ HIGH to High Z <sup>[7, 8]</sup> |                  | 5   | ns      |
| $t_{PU}^{[9]}$                         | $\overline{CE}$ LOW to Power-Up                  | 0                |     | ns      |
| $t_{PD}^{[9]}$                         | $\overline{CE}$ HIGH to Power-Down               |                  | 10  | ns      |
| <b>Write Cycle</b> <sup>[10, 11]</sup> |  |                  |     |         |
| $t_{WC}$                               | Write Cycle Time                                 | 10               |     | ns      |
| $t_{SCE}$                              | $\overline{CE}$ LOW to Write End                 | 7                |     | ns      |
| $t_{AW}$                               | Address Set-Up to Write End                      | 7                |     | ns      |
| $t_{HA}$                               | Address Hold from Write End                      | 0                |     | ns      |
| $t_{SA}$                               | Address Set-Up to Write Start                    | 0                |     | ns      |
| $t_{PWE}$                              | $\overline{WE}$ Pulse Width                      | 7                |     | ns      |
| $t_{SD}$                               | Data Set-Up to Write End                         | 6                |     | ns      |
| $t_{HD}$                               | Data Hold from Write End                         | 0                |     | ns      |
| $t_{LZWE}$                             | $\overline{WE}$ HIGH to Low Z <sup>[8]</sup>     | 3                |     | ns      |
| $t_{HZWE}$                             | $\overline{WE}$ LOW to High Z <sup>[7, 8]</sup>  |                  | 5   | ns      |

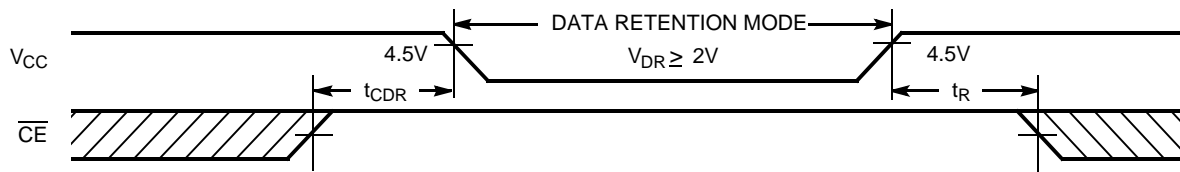
**Notes**

- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified  $I_{OL}/I_{OH}$  and 30-pF load capacitance.
- $t_{POWER}$  gives the minimum amount of time that the power supply should be at typical  $V_{CC}$  values until the first memory access can be performed.
- $t_{HZOE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  are specified with a load capacitance of 5 pF as in (c) of "AC Test Loads and Waveforms <sup>[4]</sup>" on page 4. Transition is measured when the outputs enter a high impedance state.
- At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
- This parameter is guaranteed by design and is not tested.
- The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW.  $\overline{CE}$  and  $\overline{WE}$  must be LOW to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
- The minimum write cycle time for Write Cycle no. 3 ( $\overline{WE}$  controlled,  $\overline{OE}$  LOW) is the sum of  $t_{HZWE}$  and  $t_{SD}$ .

**Data Retention Characteristics** (Over the Operating Range)

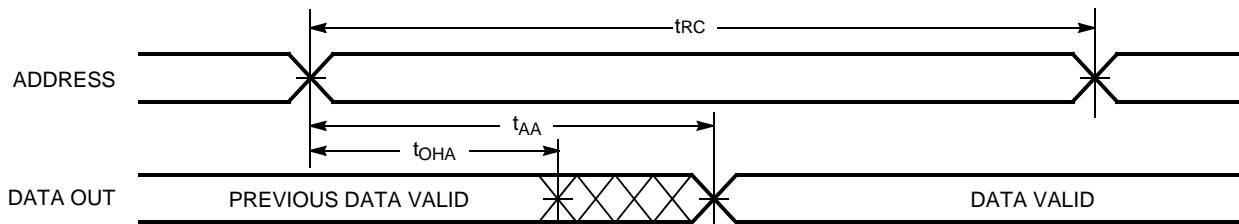
| Parameter       | Description                          | Conditions   | Min      | Max | Unit |
|-----------------|--------------------------------------|--|----------|-----|------|
| $V_{DR}$        | $V_{CC}$ for Data Retention          |  | 2.0      |     | V    |
| $I_{CCDR}$      | Data Retention Current               | $V_{CC} = V_{DR} = 2.0V$ , $\overline{CE} \geq V_{CC} - 0.3V$ ,<br>$V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$ |          | 3   | mA   |
| $t_{CDR}^{[3]}$ | Chip Deselect to Data Retention Time |  | 0        |     | ns   |
| $t_R^{[12]}$    | Operation Recovery Time              |  | $t_{RC}$ |     | ns   |

**Data Retention Waveform**

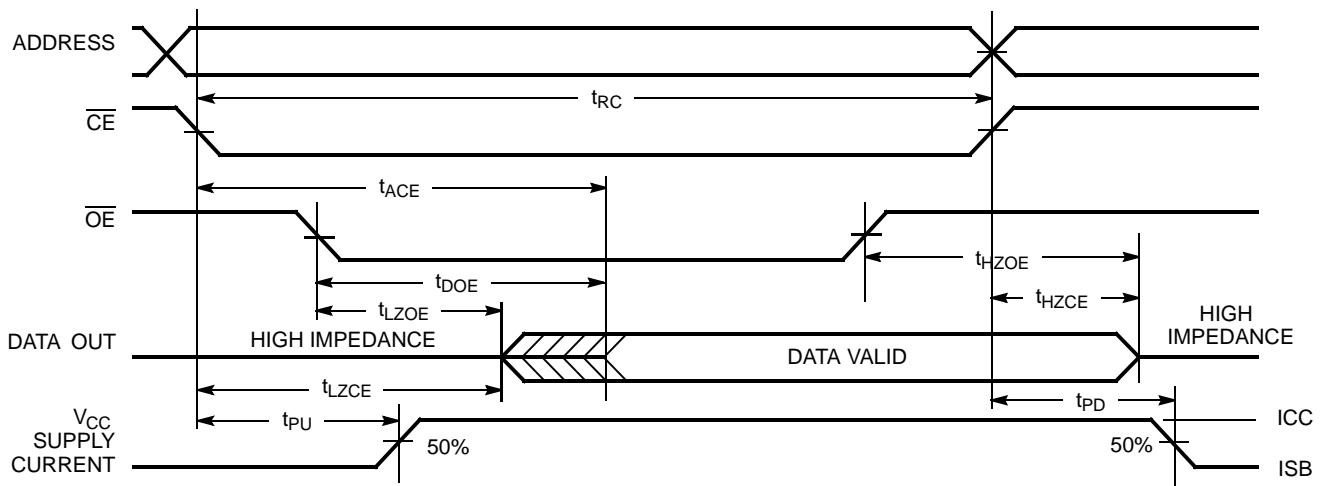


**Switching Waveforms**

**Read Cycle No. 1** (Address Transition Controlled) [13, 14]



**Read Cycle No. 2** ( $\overline{OE}$  Controlled) [14, 15]

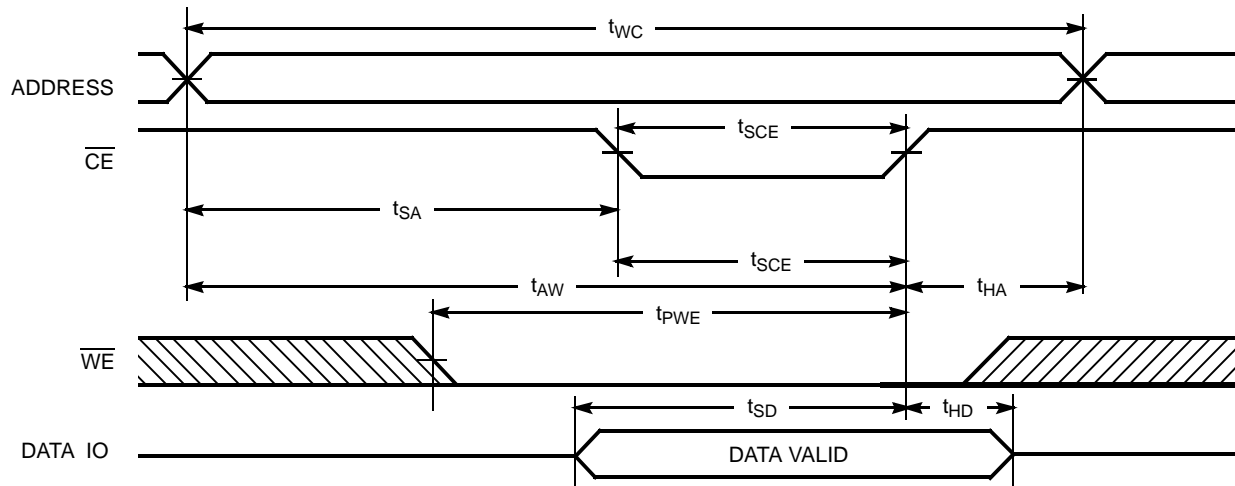


**Notes**

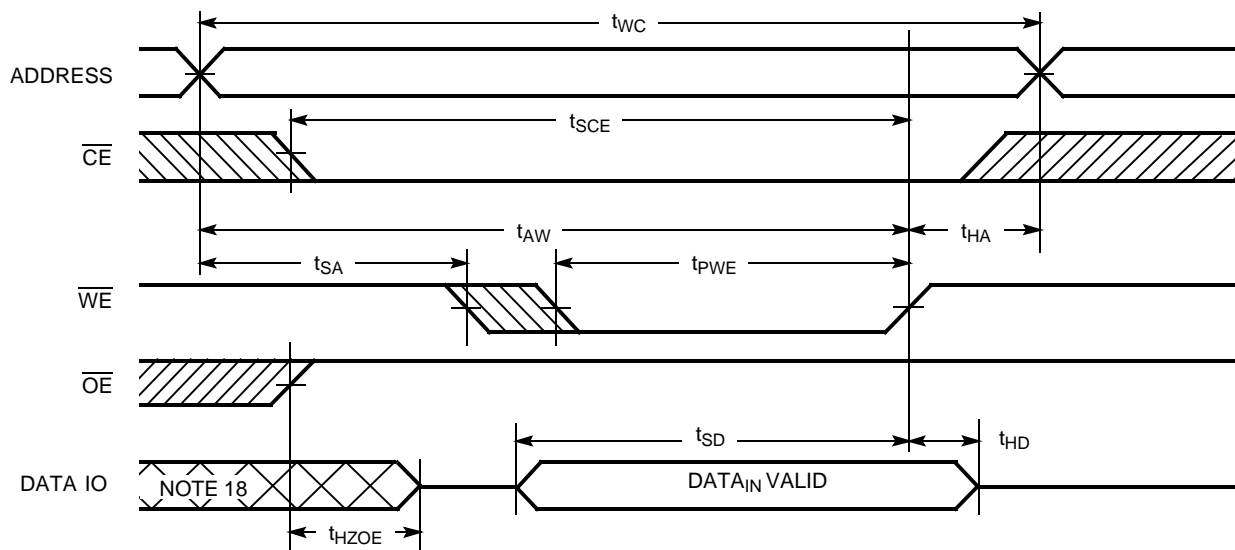
- 12. Full device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(min)} \geq 50 \mu s$  or stable at  $V_{CC(min)} \geq 50 \mu s$ .
- 13. Device is continuously selected.  $OE, CE = V_{IL}$ .
- 14.  $\overline{WE}$  is HIGH for Read cycle.
- 15. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

Switching Waveforms (continued)

Write Cycle No. 1 ( $\overline{CE}$  Controlled) [16, 17]



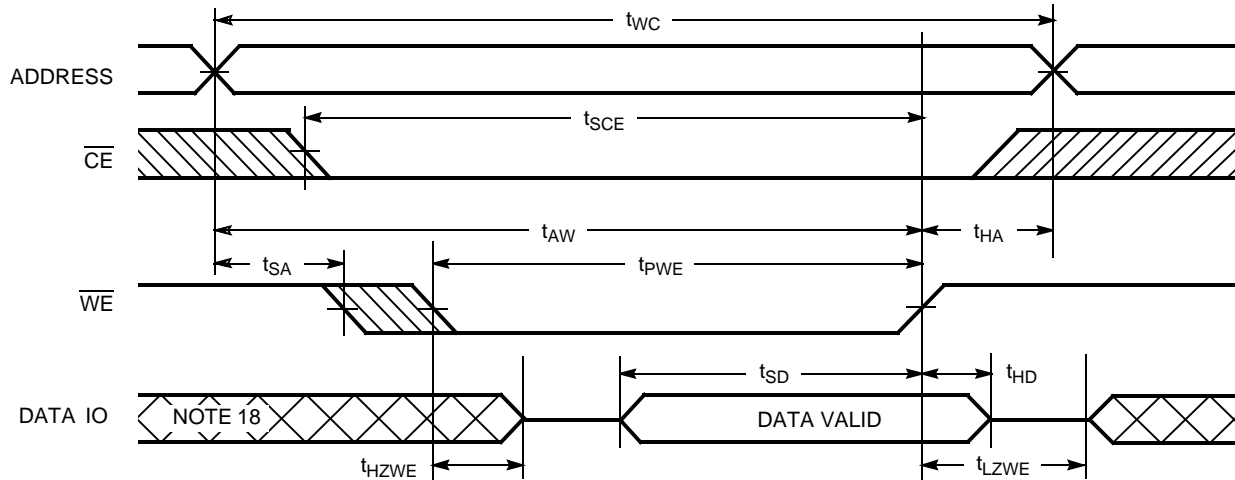
Write Cycle No. 2 ( $\overline{WE}$  Controlled,  $\overline{OE}$  HIGH During Write) [16, 17]



Notes

- 16. Data IO is high impedance if  $\overline{OE} = V_{IH}$ .
- 17. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  going HIGH, the output remains in a high-impedance state.
- 18. During this period the IOs are in the output state and input signals should not be applied.

**Switching Waveforms** (continued)

**Write Cycle No. 3** ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW) [11, 17]

**Truth Table**

| $\overline{CE}$ | $\overline{OE}$ | $\overline{WE}$ | $IO_0$ - $IO_7$ | Mode                       | Power                |
|-----------------|-----------------|-----------------|-----------------|----------------------------|----------------------|
| H               | X               | X               | High Z          | Power-Down                 | Standby ( $I_{SB}$ ) |
| L               | L               | H               | Data Out        | Read                       | Active ( $I_{CC}$ )  |
| L               | X               | L               | Data In         | Write                      | Active ( $I_{CC}$ )  |
| L               | H               | H               | High Z          | Selected, Outputs Disabled | Active ( $I_{CC}$ )  |

**Ordering Information**

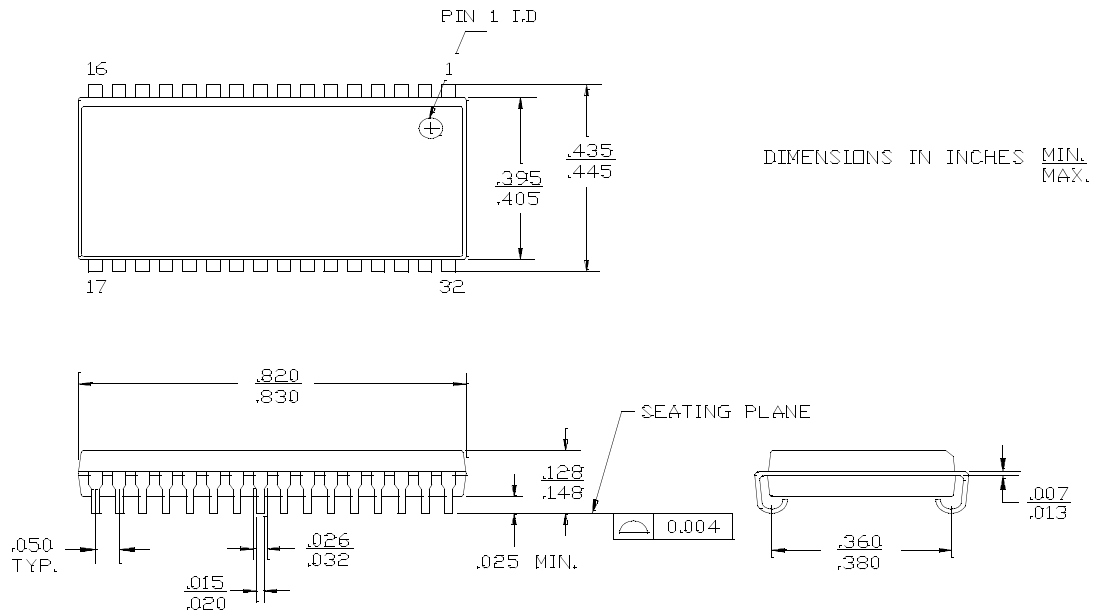
| Speed (ns) | Ordering Code    | Package Diagram | Package Type                          | Operating Range |
|------------|------------------|-----------------|---------------------------------------|-----------------|
| 10         | CY7C1019D-10VXI  | 51-85033        | 32-pin (400-Mil) Molded SOJ (Pb-free) | Industrial      |
|            | CY7C1019D-10ZSXI | 51-85095        | 32-pin TSOP Type II (Pb-free)         |                 |

Please contact your local Cypress sales representative for availability of these parts.



Package Diagrams

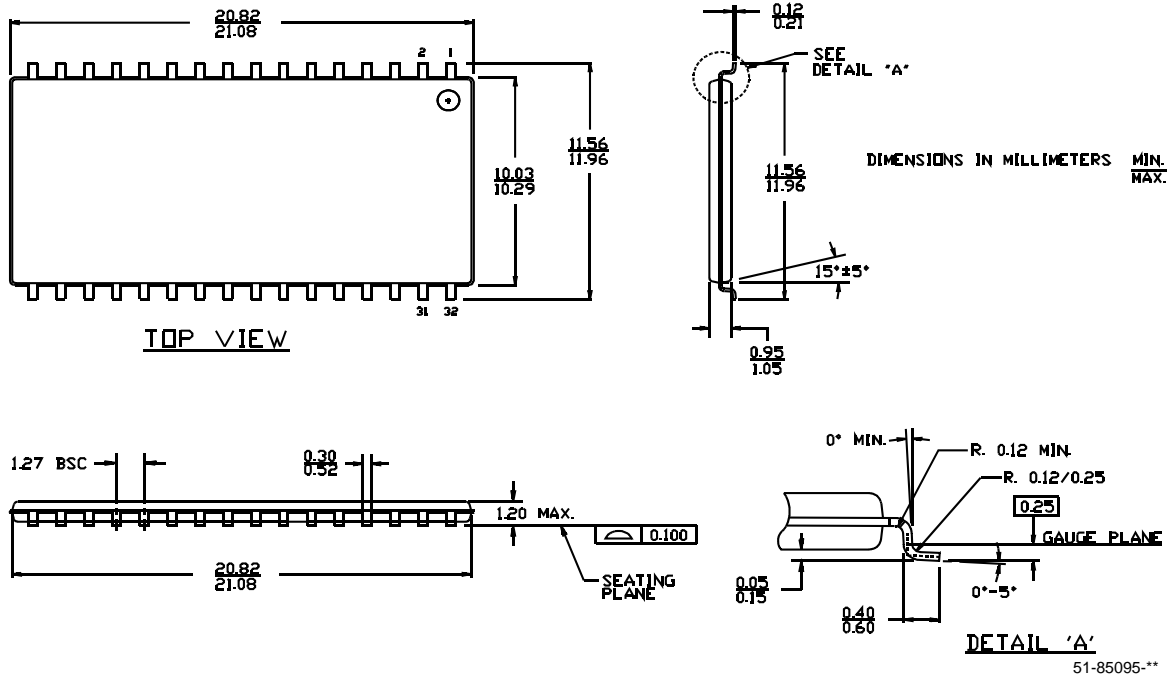
Figure 1. 32-pin (400-Mil) Molded SOJ (51-85033)



51-85033\*B

Package Diagrams (continued)

Figure 2. 32-pin Thin Small Outline Package Type II (51-85095)



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**Document History Page**

| Document Title: CY7C1019D, 1-Mbit (128K x 8) Static RAM<br>Document Number: 38-05464 |         |            |                 |  |
|--|---------|------------|-----------------|--|
| REV.   | ECN NO. | Issue Date | Orig. of Change | Description of Change  |
| **   | 201560  | See ECN    | SWI             | Advance Information data sheet for C9 IPP  |
| *A   | 233715  | See ECN    | RKF             | DC parameters are modified as per EROS (Spec # 01-2165)<br>Pb-free offering in the Ordering Information  |
| *B   | 262950  | See ECN    | RKF             | Added T <sub>power</sub> Spec in Switching Characteristics table<br>Added Data Retention Characteristics table and waveforms<br>Shaded Ordering Information  |
| *C   | 307598  | See ECN    | RKF             | Reduced Speed bins to -10 and -12 ns   |
| *D   | 520647  | See ECN    | VKN             | Converted from Preliminary to Final<br>Removed Commercial Operating range<br>Removed 12 ns speed bin<br>Added I <sub>CC</sub> values for the frequencies 83MHz, 66MHz and 40MHz<br>Updated Thermal Resistance table<br>Updated Ordering Information Table<br>Changed Overshoot spec from V <sub>CC</sub> +2V to V <sub>CC</sub> +1V in footnote #2 |
| *E   | 802877  | See ECN    | VKN             | Changed I <sub>CC</sub> spec from 60 mA to 80 mA for 100MHz, 55 mA to 72 mA for 83MHz, 45 mA to 58 mA for 66MHz, 30 mA to 37 mA for 40MHz  |