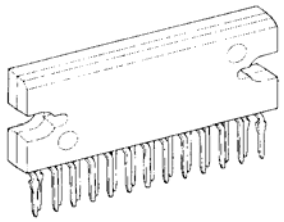
TOSHIBA BiCD Integrated Circuit Silicon Monolithic

TB6560AHQ,TB6560AFG

PWM Chopper-Type bipolar
Stepping Motor Driver IC

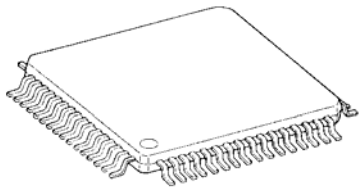
The TB6560AHQ/AFG is a PWM chopper-type sinusoidal micro-step bipolar stepping motor driver IC.
It supports both 2-phase/1-2-phase/2W1-2-phase/4W1-2-phase excitation mode and forward/reverse mode and is capable of low-vibration, high-performance drive of 2-phase bipolar type stepping motors using only a clock signal.

TB6560AHQ



HZIP25-P-1.27

TB6560AFG



HQFP64-P-1010-0.50

Weight:
HZIP25-P-1.27: 9.86 g (typ.)
HQFP64-P-1010-0.50: 0.26 g (typ.)

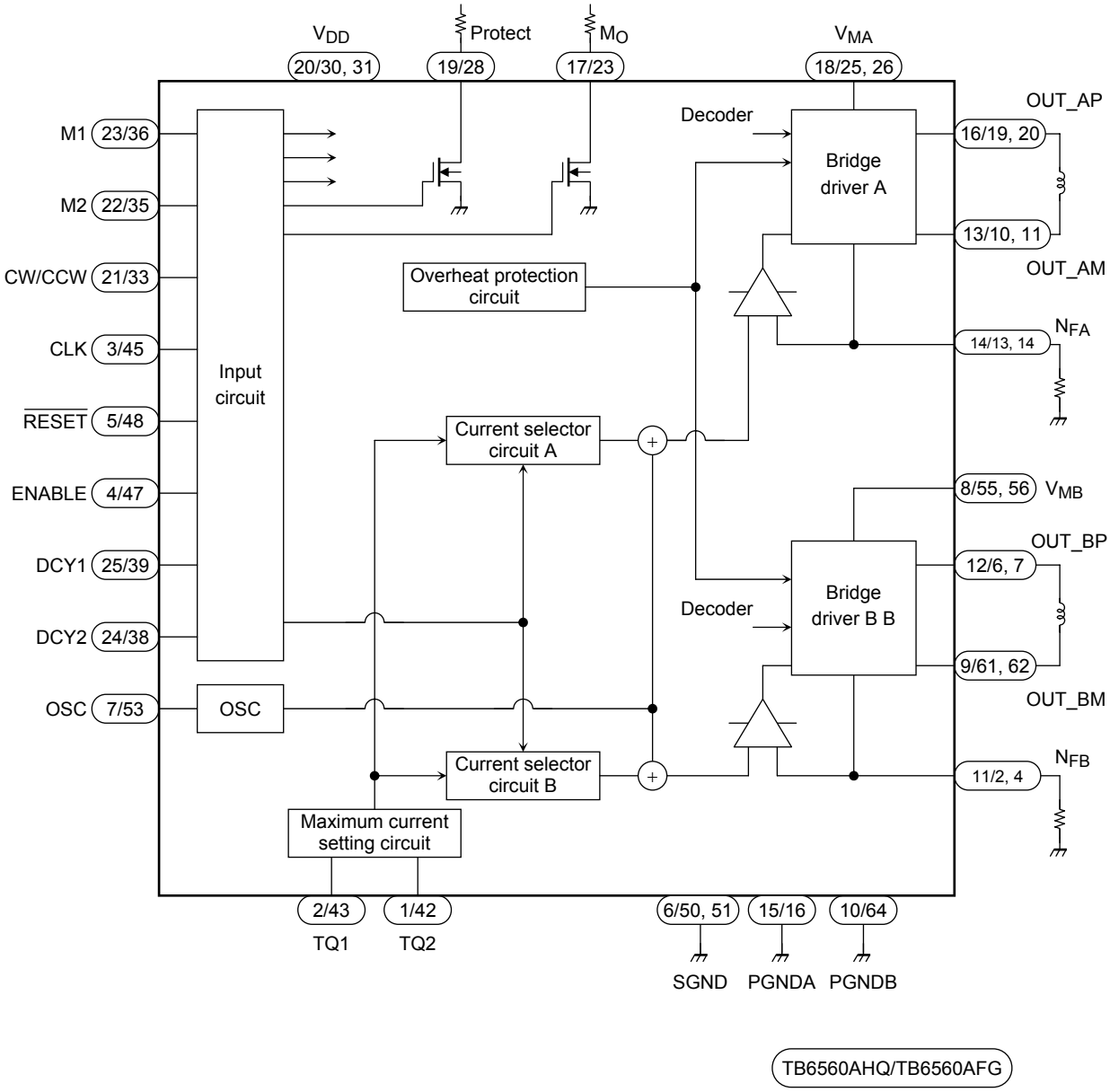
Features

- Single-chip bipolar sinusoidal micro-step stepping motor driver
- Uses high withstand voltage BiCD process:
  Ron (upper, lower) = 0.6 Ω (typ.)
- Forward and reverse rotation control available
- Selectable phase drive (2, 1-2, 2W1-2, and 4W1-2)
- High output withstand voltage: VDSS = 40 V
- High output current: I_{OUT} = AHQ: 3.5 A (peak)
  AFG: 2.5 A (peak)
- Packages: HZIP25-P-1.27/HQFP64-P-1010-0.50
- Built-in input pull-down resistor: 100 kΩ (typ.)
- Output monitor pin equipped: MO current (I_{MO} (max) = 1 mA)
- Equipped with reset and enable pins
- Built-in overheat protection circuit

The TB6560AFG is RoHS compatible.
The TB6560AHQ is a Sn-plated product including Pb which is RoHS exempted.
The following conditions apply to solderability:
*Solderability
1. Use of Sn-37Pb solder bath
   *solder bath temperature = 230°C
   *dipping time = 5 seconds
   *number of times = once
   *use of R-type flux
2. Use of Sn-3.0Ag-0.5Cu solder bath
   *solder bath temperature = 245°C
   *dipping time = 5 seconds
   *the number of times = once
   *use of R-type flux

*: Since this product has a MOS structure, it is sensitive to electrostatic discharge. These ICs are highly sensitive to electrostatic discharge. When handling them, please be careful of electrostatic discharge, temperature and humidity conditions.

Block Diagram



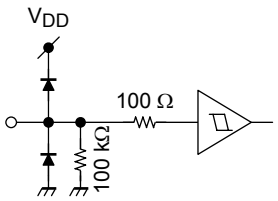
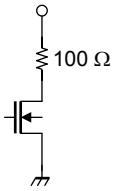
Pin Functions

Pin No.		I/O	Symbol	Functional Description
AHQ	AFG			
1	42	Input	TQ2	Torque setting input (current setting)
2	43	Input	TQ1	Torque setting input (current setting)
3	45	Input	CLK	Step transition, clock input
4	47	Input	ENABLE	H: Enable; L: All output OFF
5	48	Input	$\overline{\text{RESET}}$	L: Reset (output is reset to its initial state)
6	50/51	—	SGND	Signal ground (control side) (Note 1)
7	53	—	OSC	Connects to and oscillates CR. Output chopping.
8	55/56	Input	V_{MB}	Motor side power pin (B phase side) (Note 1)
9	61/62	Output	OUT_BM	OUT_B output (Note 1)
10	64(*)	—	PGNDB	Power ground
11	2/4(*)	—	N_{FB}	B channel output current detection pin (resistor connection). Short the two pins for AFG. (Note 1)
12	6/7	Output	OUT_BP	OUT_B output (Note 1)
13	10/11	Output	OUT_AM	OUT_A output (Note 1)
14	13/14(*)	—	N_{FA}	A channel output current detection pin (resistor connection). Short the two pins for AFG. (Note 1)
15	16	—	PGNDA	Power ground
16	19/20	Output	OUT_AP	OUT_A output (Note 1)
17	23	Output	M_O	Initial state detection output. ON when in initial state
18	25/26	Input	V_{MA}	Motor side power pin (A phase side) (Note 1)
19	28	Output	Protect	When TSD, ON. Normal Z.
20	30/31	Input	V_{DD}	Control side power pin. (Note 1)
21	33	Input	CW/CCW	Forward/Reverse toggle pin. L: Forward; H: Reverse
22	35	Input	M2	Excitation mode setting input
23	36	Input	M1	Excitation mode setting input
24	38	Input	DCY2	Current Decay mode setting input
25	39	Input	DCY1	Current Decay mode setting input

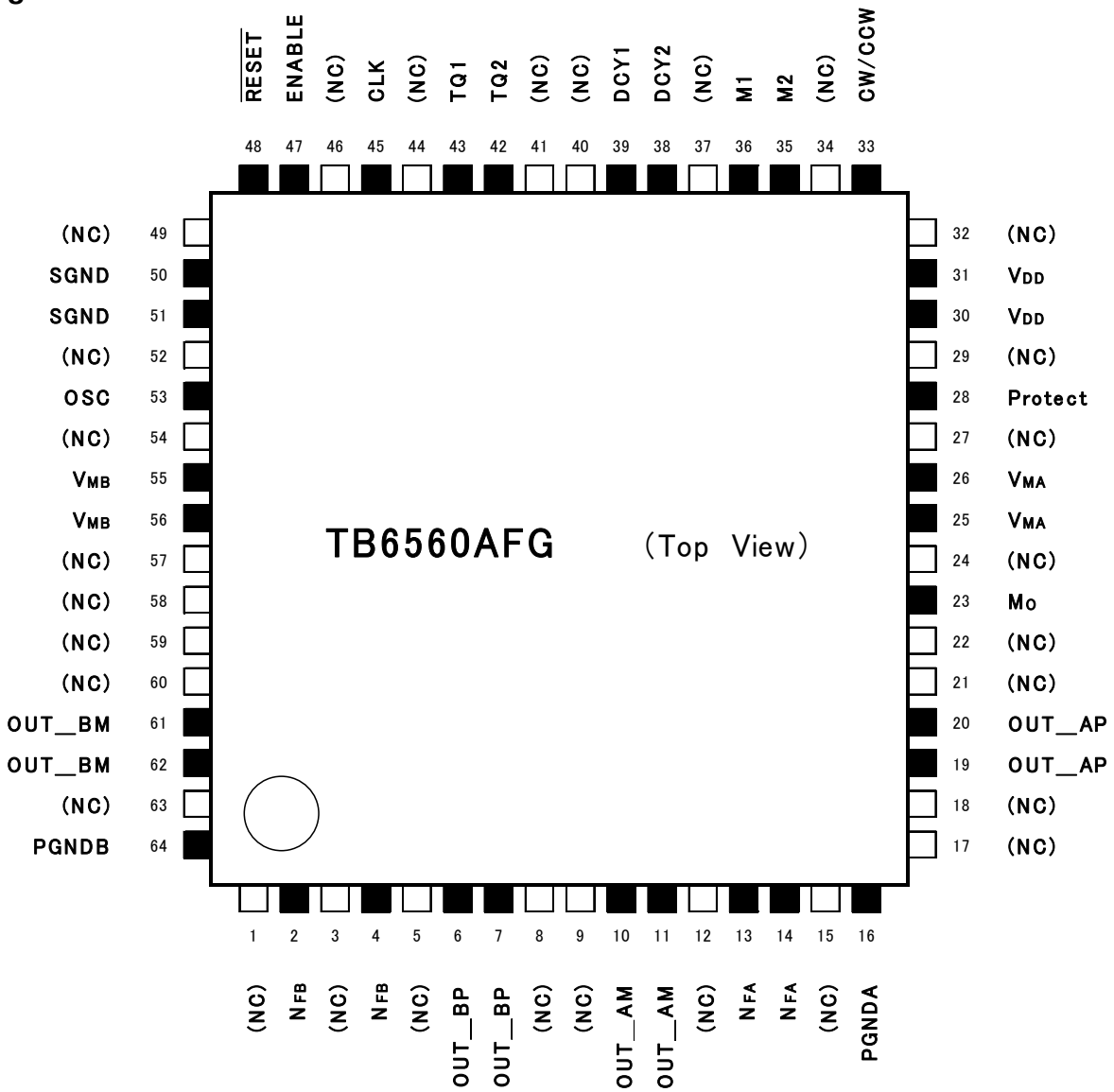
- (*) : Pin assignment of TB6560AFG is different from that of TB6560FG.
- TB6560AHQ: No Non-connection (NC)
- TB6560AFG: Other than the above pins, all are NC. Pin numbers of NC are 1, 3, 5, 8, 9, 12, 15, 17, 18, 21, 22, 24, 27, 29, 32, 34, 37, 40, 41, 44, 46, 49, 52, 54, 57, 58, 59, 60, and 63.
- No problem to apply the voltage because of no connection of NC and Pin internally.
- All control input pins: Pull-down resistor 100 kΩ (typ.)

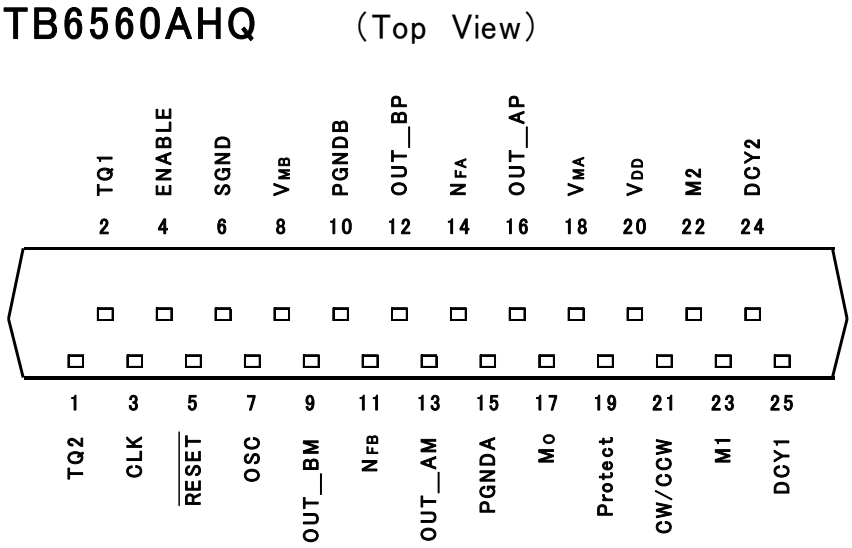
Note 1: If the TB6560AFG pin number column indicates more than one pin, the indicated pins should be tied to each other at a position as close to the pins as possible.
(The electrical characteristics of the relevant pins in this document refer to those when they are handled in that way.)

<Terminal circuits>

Input pins (M1, M2, CLK, CW/CCW, ENABLE and RESET)	Output ins (MO, PROTECT)
	

Pin Assignment





Absolute Maximum Ratings (Ta = 25°C)

Characteristic			Symbol	Rating	Unit
Power supply voltage			V_{DD}	6	V
			$V_{MA/B}$	40	
Output current	Peak	AHQ	$I_{O\ (PEAK)}$	3.5	A/phase
		AFG		2.5	
MO drain current			$I_{(MO)}$	1	mA
Input voltage			V_{IN}	5.5	V
Power dissipation		AHQ	P_D	5 (Note 1)	W
				43 (Note 2)	
		AFG		1.7 (Note 3)	
				4.2 (Note 4)	
Operating temperature			T_{opr}	−30 to 85	°C
Storage temperature			T_{stg}	−55 to 150	°C

Note 1: Ta = 25°C, No heat sink.

Note 2: Ta = 25°C, with infinite heat sink (HZIP25).

Note 3: Ta = 25°C, with soldered leads.

Note 4: Ta = 25°C, when mounted on the board (4-layer board).

Operating Range (Ta = −30 to 85°C)

Characteristic		Symbol	Test Condition	Min	Typ.	Max	Unit
Power supply voltage		V_{DD}	—	4.5	5.0	5.5	V
		$V_{MA/B}$	$V_{MA/B} \geqq V_{DD}$	4.5	—	34	V
Output current	AHQ	I_{OUT}	—	—	—	3	A
	AFG			—	—	1.5	
Input voltage		V_{IN}	—	0	—	5.5	V
Clock frequency		f_{CLK}	—	—	—	15	kHz
OSC frequency		f_{OSC}	—	—	—	600	kHz

Electrical Characteristics (Ta = 25°C, V_{DD} = 5 V, V_M = 24 V)

Characteristic		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Input voltage	High	$V_{IN\ (H)}$	1	M1, M2, CW/CCW, CLK, $\overline{RESET}$, ENABLE, DECAY, TQ1, TQ2, ISD	2.0	—	V_{DD}	V
	Low	$V_{IN\ (L)}$			−0.2	—	0.8	
Input hysteresis voltage		V_H	1		—	400	—	mV
Input current		$I_{IN\ (H)}$	1	M1, M2, CW/CCW, CLK, $\overline{RESET}$, ENABLE, DECAY, TQ1, TQ2, ISD V_{IN} = 5.0 V Built-in pull-down resistor	30	55	80	μA
		$I_{IN\ (L)}$		V_{IN} = 0 V	—	—	1	
Consumption current V_{DD} pin		I_{DD1}	1	Output open, $\overline{RESET}$: H, ENABLE: H (2, 1-2 phase excitation)	—	3	5	mA
		I_{DD2}		Output open, $\overline{RESET}$: H, ENABLE: H (W1−2, 2W1-2 phase excitation)	—	3	5	
		I_{DD3}		$\overline{RESET}$: L, ENABLE: L	—	2	5	
		I_{DD4}		$\overline{RESET}$: H, ENABLE: L	—	2	5	
Consumption current V_M pin		I_{M1}	1	$\overline{RESET}$: H/L, ENABLE: L	—	0.5	1	mA
		I_{M2}		$\overline{RESET}$: H/L, ENABLE: H	—	0.7	2	
Output channel margin of error		ΔV_O	—	B/A, C_{OSC} = 330 μF	−5	—	5	%
VNF level Level differential		V_{NFHH}	—	TQ1 = H, TQ2 = H	10	20	30	%
		V_{NFHL}		TQ1 = L, TQ2 = H	47	50	55	
		V_{NFLH}		TQ1 = H, TQ2 = L	70	75	80	
		V_{NFLL}		TQ1 = L, TQ2 = L			100	
Minimum clock pulse width		$t_{W\ (CLK)}$	—	C = 330 pF	30	—	—	μs
MO output residual voltage		V_{OL} MO	—	I_{OL} = 1 mA	—	—	0.5	V
TSD (Note)		TSD	—		—	170	—	°C
TSD hysteresis (Note)		TSDhys	—		—	20	—	°C
Oscillating frequency		f_{OSC}	—	C = 330 pF	60	130	200	kHz

Note: No shipping test

Electrical Characteristics (Ta = 25°C, V_{DD} = 5 V, V_M = 24 V)

Characteristic				Symbol	Test Circuit	Test Condition		Min	Typ.	Max	Unit
Output ON resistor			AHQ	Ron_{U1H}	4	I_{OUT} = 1.5 A		—	0.3	0.4	Ω
				Ron_{L1H}				—	0.3	0.4	
			AFG	Ron_{U1F}		I_{OUT} = 1.5 A		—	0.35	0.5	
				Ron_{L1F}				—	0.35	0.5	
A-B chopping current (Note 1)	4W1-2-phase excitation	2W1-2-phase excitation	1-2-phase excitation	Vector	—	θ = 0	TQ1 = L, TQ2 = L	—	100	—	%
		—	—			θ = 1/16		—	100	—	
		2W1-2-phase excitation	—			θ = 2/16		93	98	100	
		—	—			θ = 3/16		91	96	100	
		2W1-2-phase excitation	—			θ = 4/16		87	92	97	
		—	—			θ = 5/16		83	88	93	
		2W1-2-phase excitation	—			θ = 6/16		78	83	88	
		—	—			θ = 7/16		72	77	82	
		2W1-2-phase excitation	1-2-phase excitation			θ = 8/16		66	71	76	
		—	—			θ = 9/16		58	63	68	
		2W1-2-phase excitation	—			θ = 10/16		51	56	61	
		—	—			θ = 11/16		42	47	52	
		2W1-2-phase excitation	—			θ = 12/16		33	38	43	
		—	—			θ = 13/16		24	29	34	
		2W1-2-phase excitation	—			θ = 14/16		15	20	25	
		—	—			θ= 15/16		5	10	15	
	2-phase excitation					—		—	100	—	
Reference voltage				V_{NF}	—	TQ1, TQ2 = L (100%) OSC = 100 kHz		450	500	550	mV
Output transistor switching characteristics (Note 2)				t_r	7	R_L = 10 Ω, V_{NF} = 0.5 V		—	1	—	μs
				t_f				—	1	—	
Delay time (Note 2)				t_{pLH}		$\overline{RESET}$ to output		—	1	—	
				t_{pLH}		ENABLE to output		—	3	—	
				t_{pHL}				—	2	—	
Output leakage current			Upper side	I_{LH}	6	V_M = 40 V		—	—	1	μA
			Lower side	I_{LL}				—	—	1	

Note 1: Maximum current (θ = 0): 100%

Note 2: No shipping test.

Description of Functions

1. Excitation Settings

You can use the M1 and M2 pin settings to configure four different excitation settings. (The default is 2-phase excitation using the internal pull-down.)

Input		Mode (Excitation)
M2	M1	
L	L	2-phase
L	H	1-2-phase
H	L	4W1-2-phase
H	H	2W1-2-phase

2. Function

When the ENABLE signal goes Low level, it sets an OFF on the output. The output changes to the Initial mode shown in the table below when the $\overline{\text{RESET}}$ signal goes Low level. In this mode, the status of the CLK and CW/CCW pins are irrelevant.

Input				Output Mode
CLK	CW/CCW	$\overline{\text{RESET}}$	ENABLE	
↓	L	H	H	CW
↓	H	H	H	CCW
X	X	L	H	Initial mode
X	X	X	L	Z

X: Don't care

3. Initial Mode

When $\overline{\text{RESET}}$ is used, the phase currents are as follows. In this instance, the MO pin is L (connected to open drain).

Excitation Mode	A Phase Current	B Phase Current
2-phase	100%	−100%
1-2-phase	100%	0%
W1-2-phase	100%	0%
2W1-2-phase	100%	0%

4. Decay Mode Settings

Discharging time of PWM operation corresponds to four cycles of OSC frequency. 25% decay is created by inducing decay during the last cycle in Fast mode; 50% decay is created by inducing decay during the last two cycles in Fast mode; and 100% decay is created by inducing all four cycles in Fast mode.
If there is no input with the pull-down resistor connection then the setting is Normal.

Dcy2	Dcy1	Current Decay Setting
L	L	Normal 0%
L	H	25% Decay
H	L	50% Decay
H	H	100% Decay

5. Torque Settings (Current Value)

The current ratio used in actual operations is determined in regard to the current setting due to resistance.
Configure this for extremely low torque scenarios such as when Weak Excitation mode is stopped.
If there is no input with the pull-down resistor connection then the setting is 100% torque.

TQ2	TQ1	Current Ratio
L	L	100%
L	H	75%
H	L	50%
H	H	20% (weak excitation)

6. Calculating Formula of Setting Current

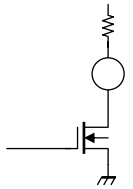
To drive at constant current, the reference current should be setup by the external resistance.
The current can not be charged when the voltage applied to NFA (B) terminal is 0.5 V or more (in case torque is 100%).
Iout(A)=0.5V/RNF(Ω)
(Ex.) Maximum current is 1A : External resistance of 0.5Ω is used.

7. Protect and MO (Output Pins)

There is an open-drain connection for the output pins. Connect the pull-up resistance in using.
When a given pin is in its designated state it will go ON and output at Low level.

Pin State	Protect	MO
Low	Overheat protection operation	Initial state
Z	Normal operation	Other than initial state

Open-drain connection



8. OSC (Setting External Condenser)

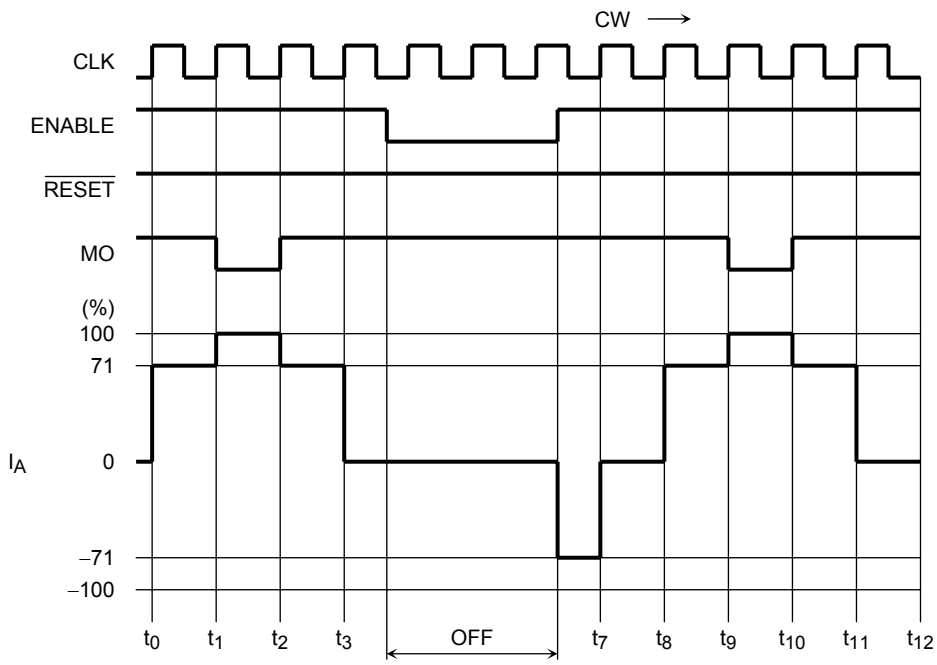
Triangle-waves are generated internally by connecting the external condenser to the OSC terminal and having the CR oscillation.
fosc = 1/(Cosc × 1.5 × (10/Cosc + 1)/66) × 1000 kHz

The approximate values are as shown below.

Condenser	Oscillating Frequency
1000 pF	44 kHz
330 pF	130 kHz
100 pF	400 kHz

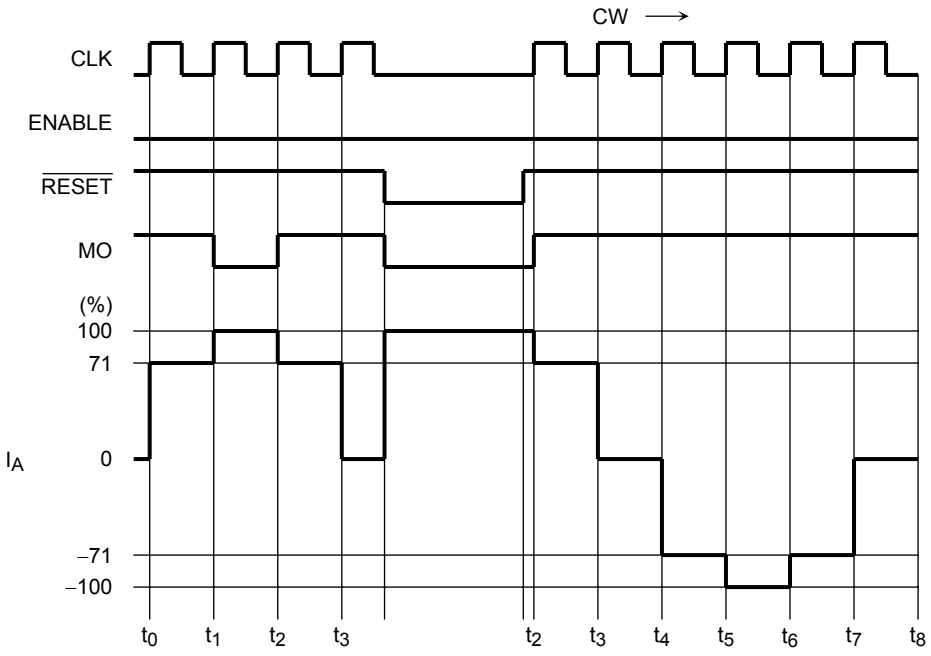
Relationship between Enable, $\overline{\text{RESET}}$ and Output (OUT and MO)

Ex-1: ENABLE 1-2-Phase Excitation (M1: H, M2: L)



The ENABLE signal at Low level disables only the output signals. Internal logic functions proceed in accordance with input clock signals and without regard to the ENABLE signal. Therefore output current is initiated by the timing of the internal logic circuit after release of disable mode.

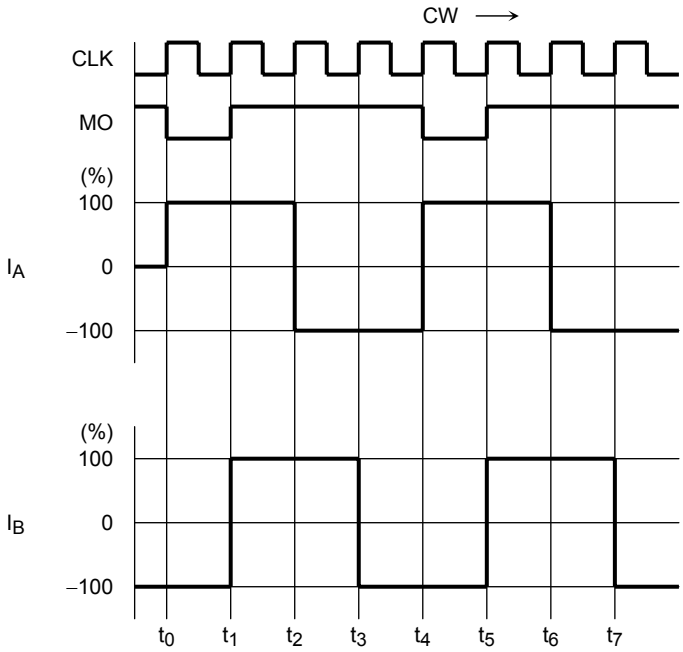
Ex-2: $\overline{\text{RESET}}$ 1-2-Phase Excitation (M1: H, M2: L)



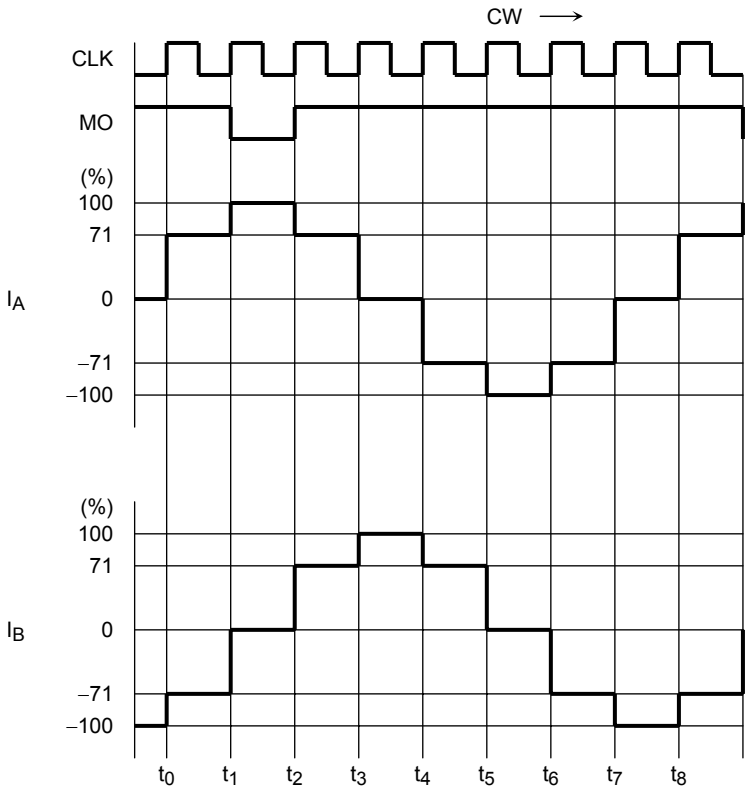
When the $\overline{\text{RESET}}$ signal goes Low level, output goes Initial state and the MO output goes Low level (Initial state: A Channel output current is 100%).

Once the $\overline{\text{RESET}}$ signal returns to High level, output continues from the next state after Initial from the next raise in the Clock signal.

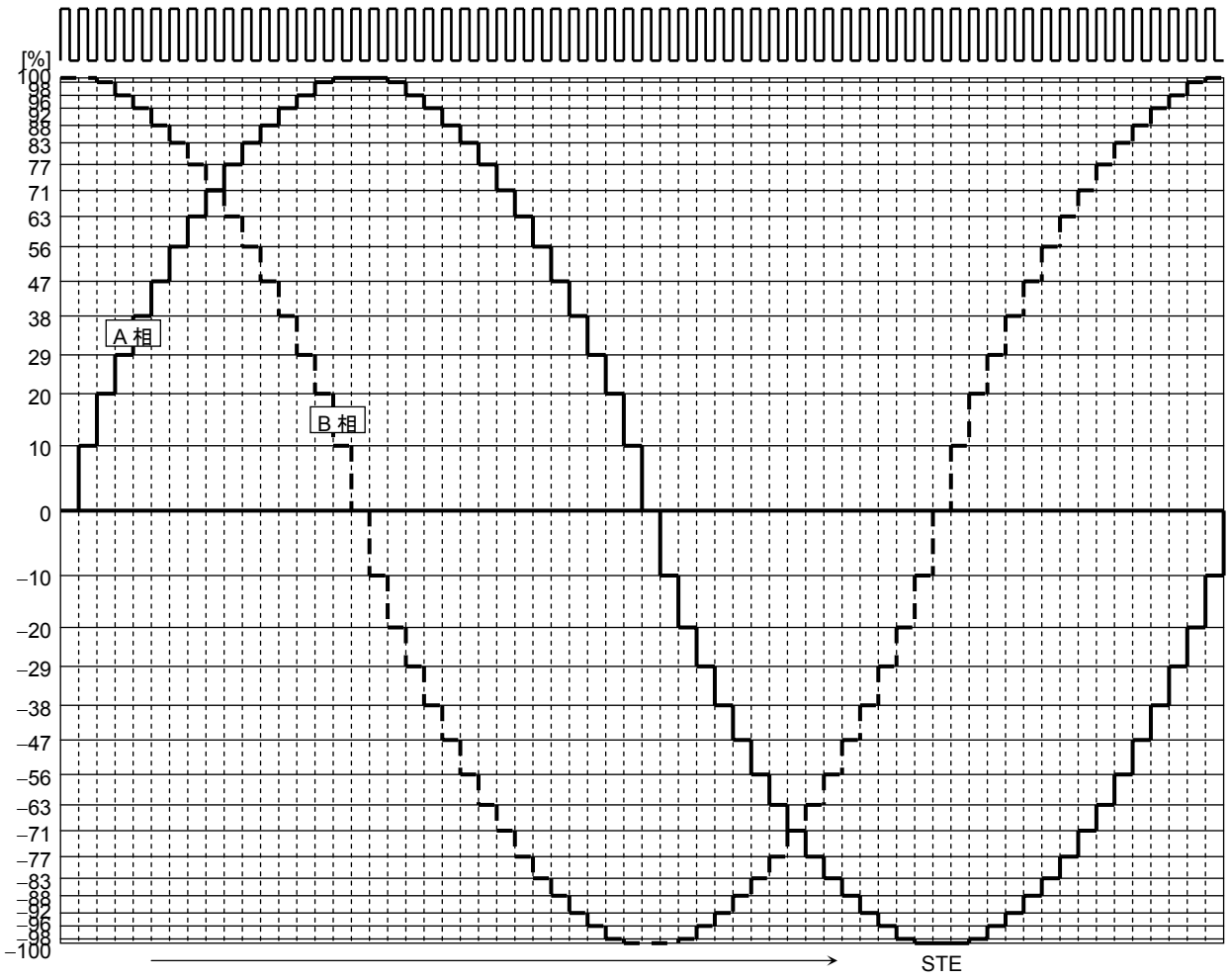
2-Phase Excitation (M1: L, M2: L, CW Mode)



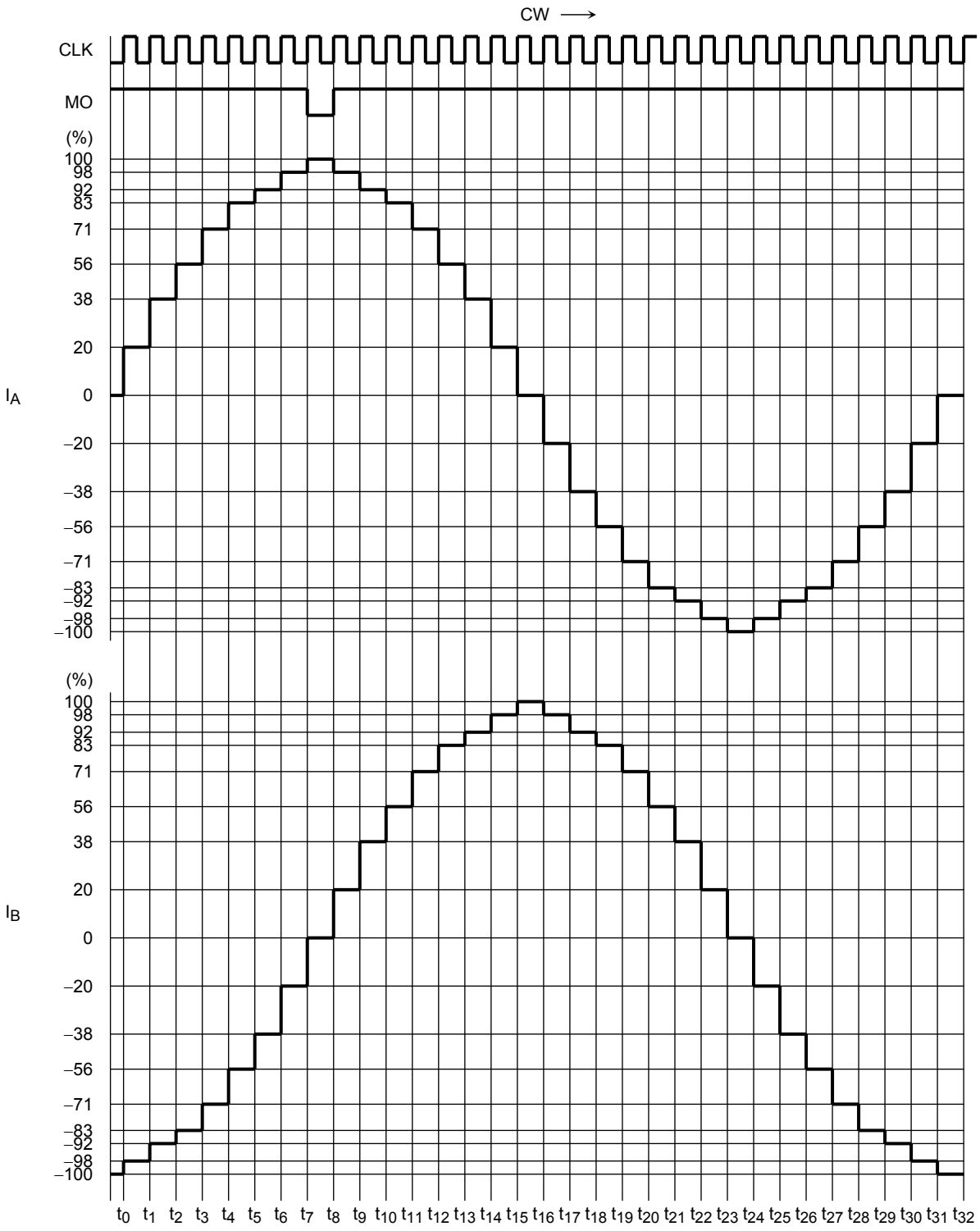
1-2-Phase Excitation (M1: H, M2: L, CW Mode)



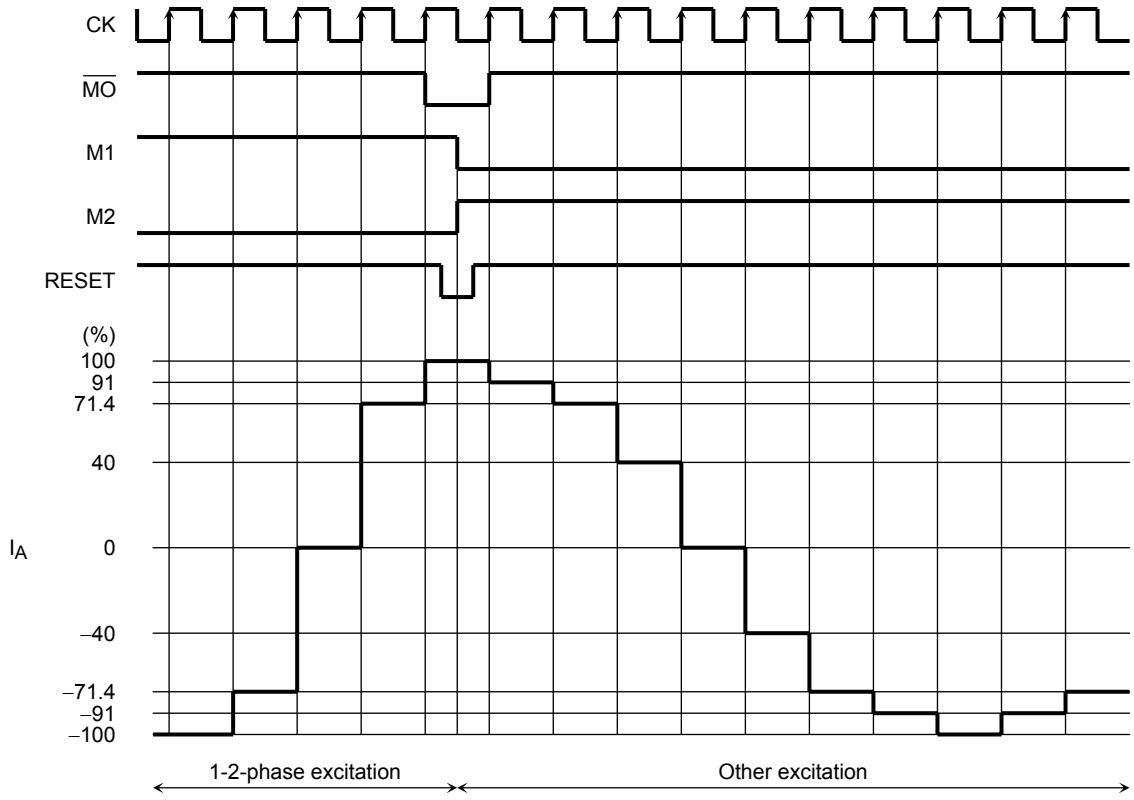
4W1-2-Phase Excitation (M1: L, M2: H, CW Mode)



2W1-2-Phase Excitation (M1: H, M2: H, CW Mode)



<Input Signal Example>



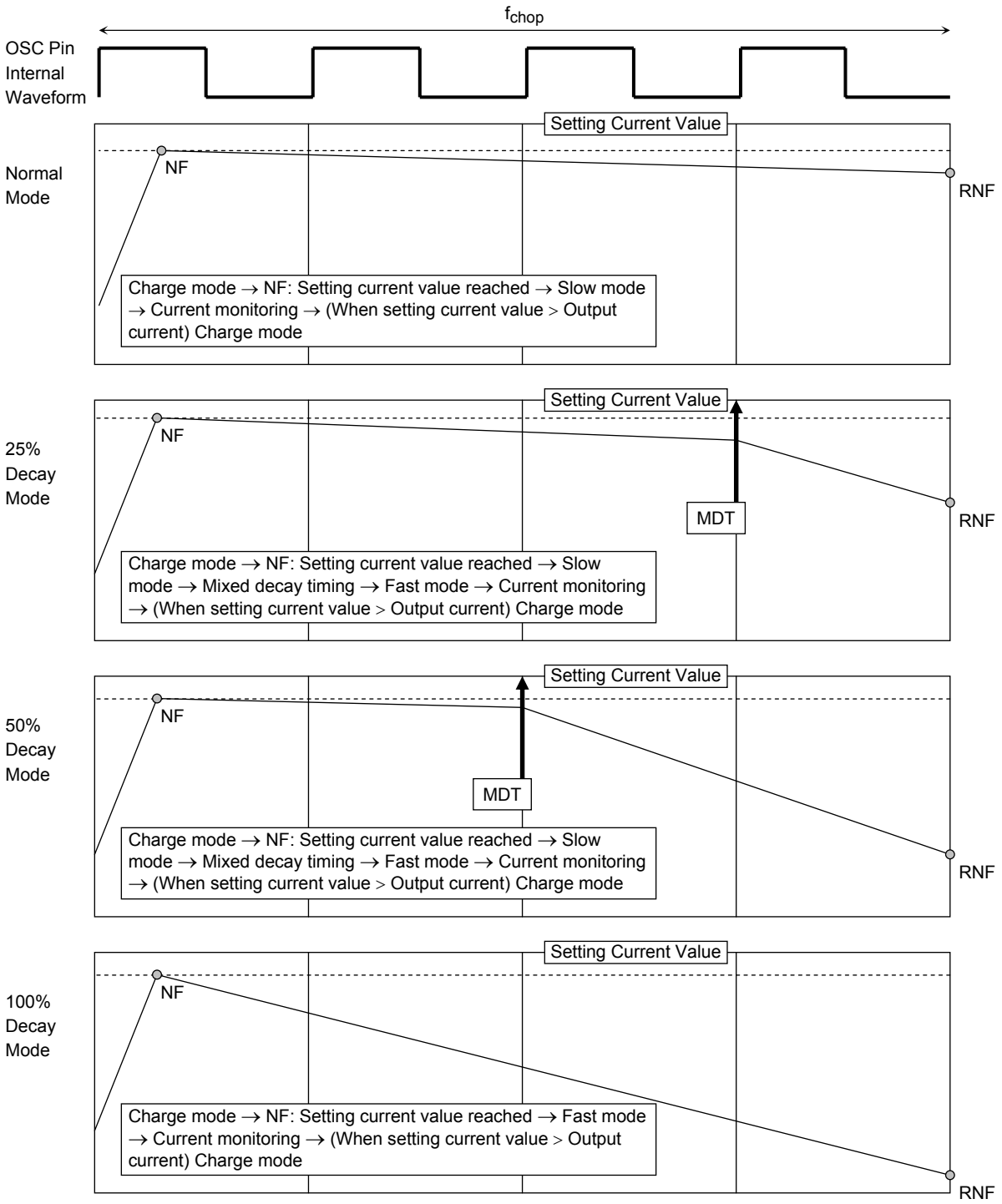
As for the change of M1 and M2, it is recommended that M1 and M2 signals be changed after setting the RESET signal Low during the Initial state (MO is Low). Even when the MO is Low, changing the RESET signal without setting the RESET signal Low may cause the discontinuity in the current waveform.

1. Current Waveform and Settings of Mixed Decay Mode

You can configure the points of the current's shaped width (current's pulsating flow) using 1-bit input in Decay mode for constant-current control.

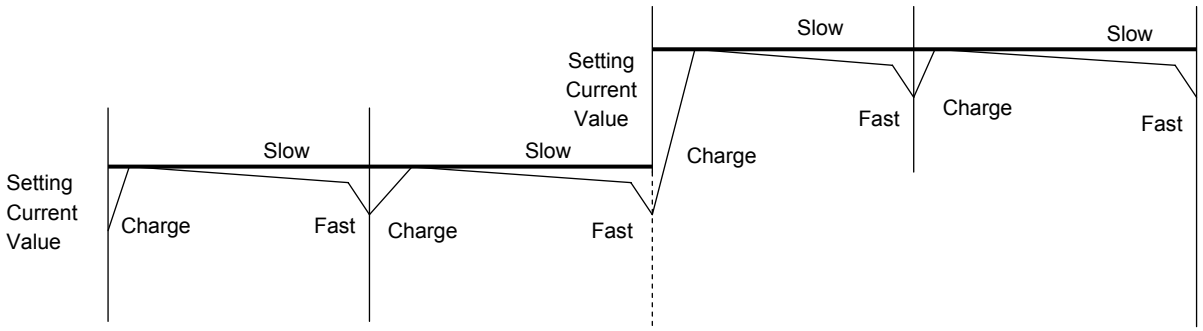
"NF" refers to the point at which the output current reaches its setting current value and "RNF" refers to the monitoring timing of the setting current.

The smaller the MDT value, the smaller the current ripple (current wave peak), and the current's decay capability will fall.

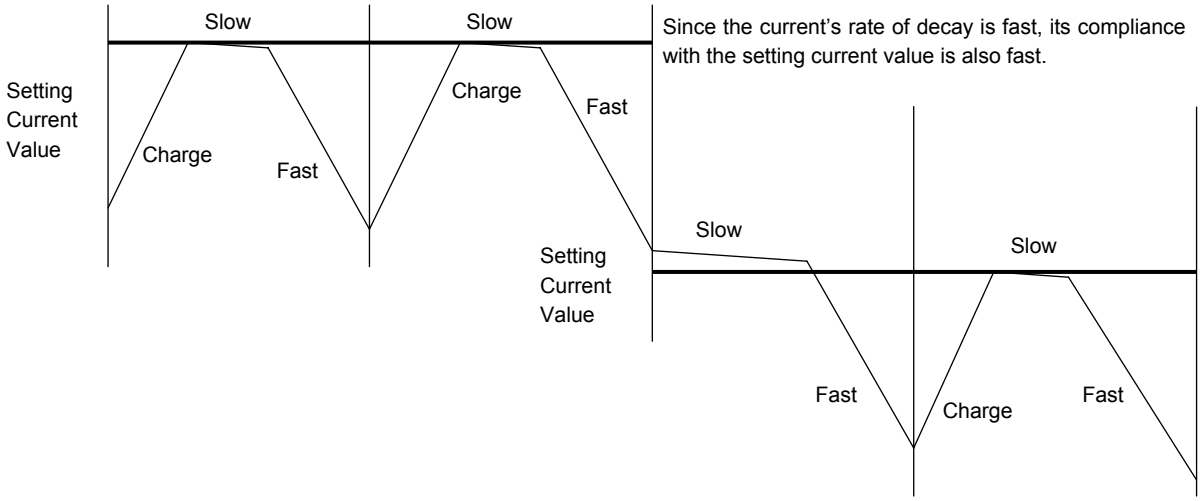


2. Current Control Modes (Decay Mode effect)

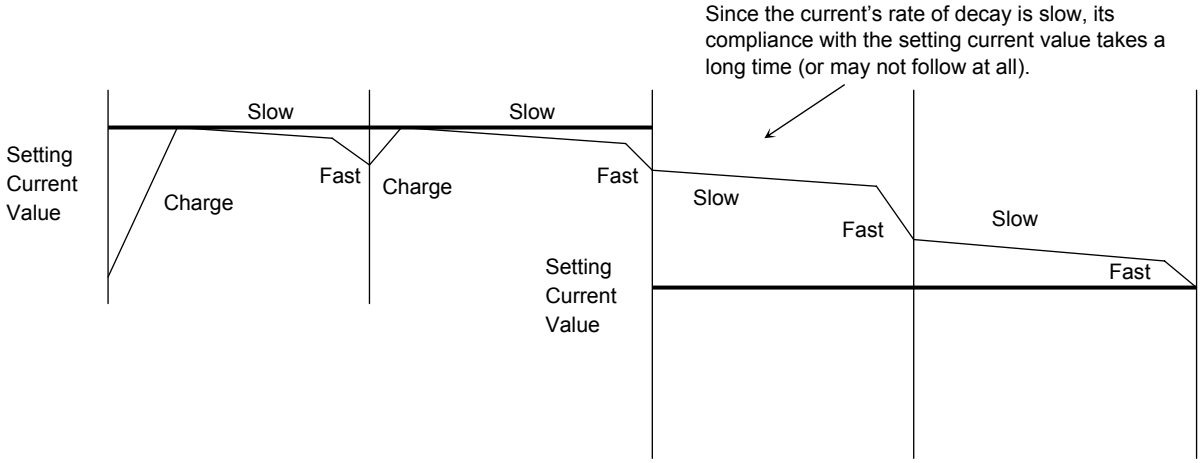
- Direction in which current value increases (sine wave)



- Direction in which sine wave decreases
  (when a high decay ratio (MDT%) is used in Mixed Decay mode)



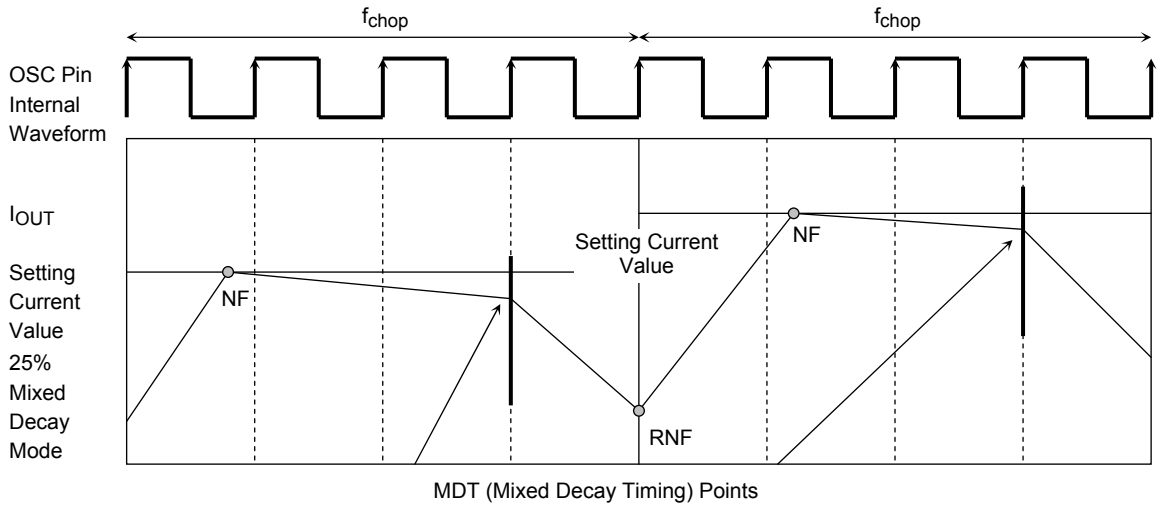
- Direction in which sine wave decreases
  (when a low decay ratio (MDT%) is used in Mixed Decay mode)



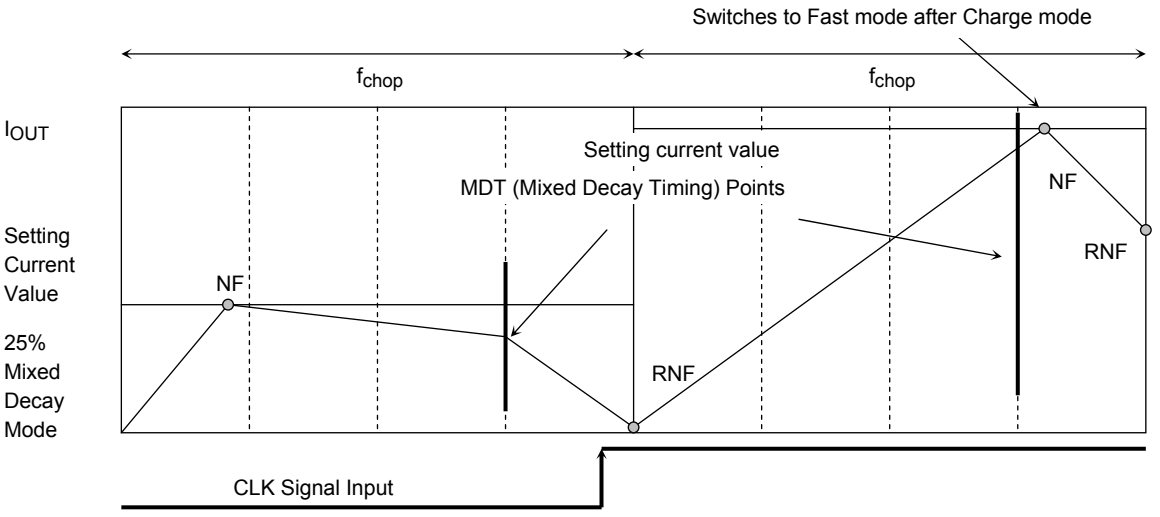
During Mixed Decay mode and Fast Decay mode, if the setting current value < output current at RNF: current monitoring point, the Charge mode at the next chopping cycle will disappear and the pattern will change to Slow, Fast Mode (Slow → Fast occurs at MDT). (In reality, a charge is applied momentarily to confirm the current.)

Note: These figures are intended for illustrative purposes only. If designed more realistically, they would show transient response curves.

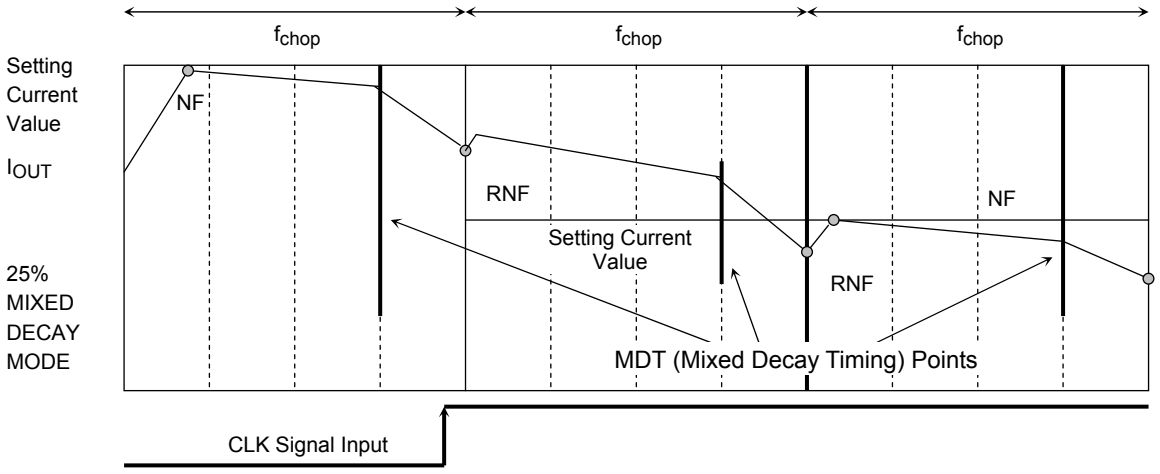
3. Mixed Decay Mode Waveform (Current Waveform)



- When the NF points come after mixed decay timing



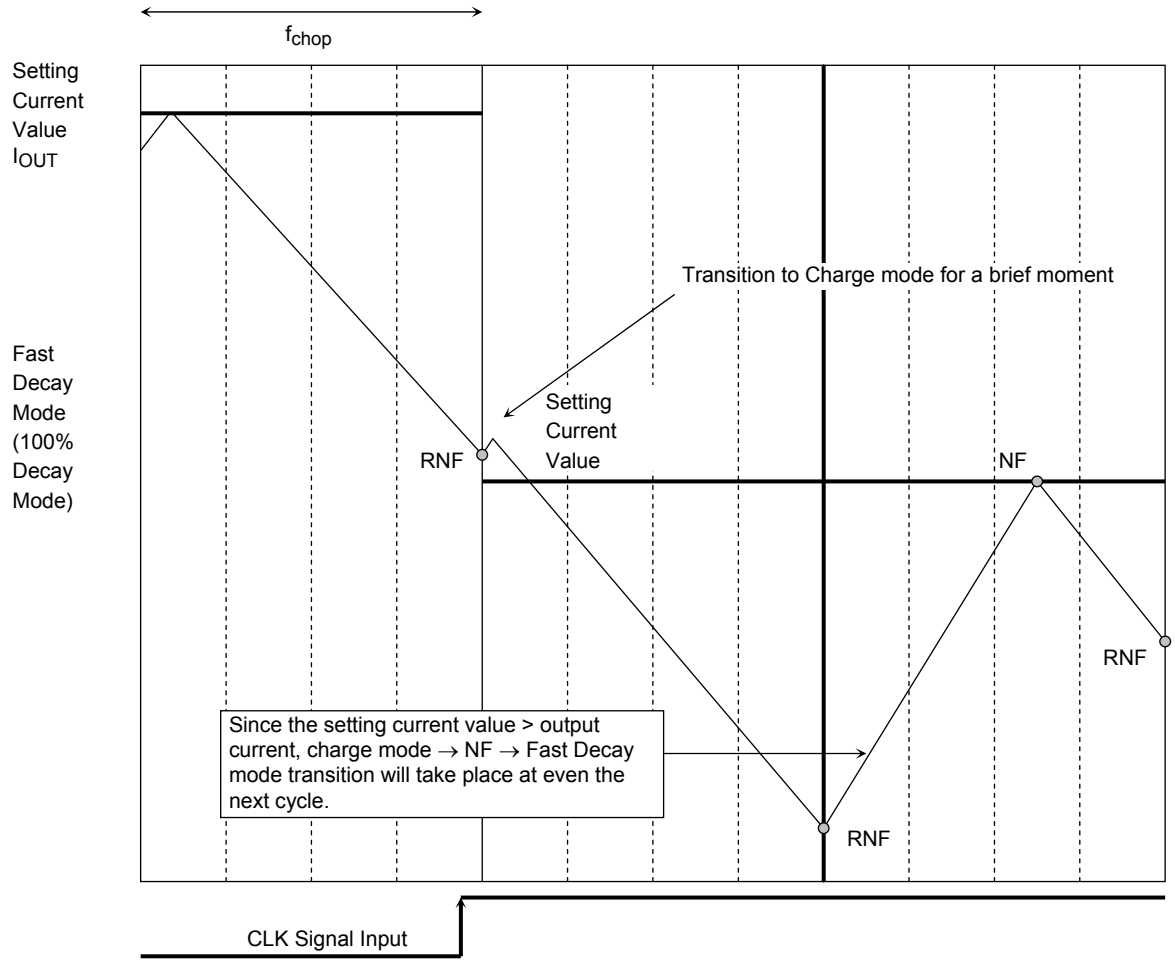
- When the output current value > Setting current value in mixed decay mode



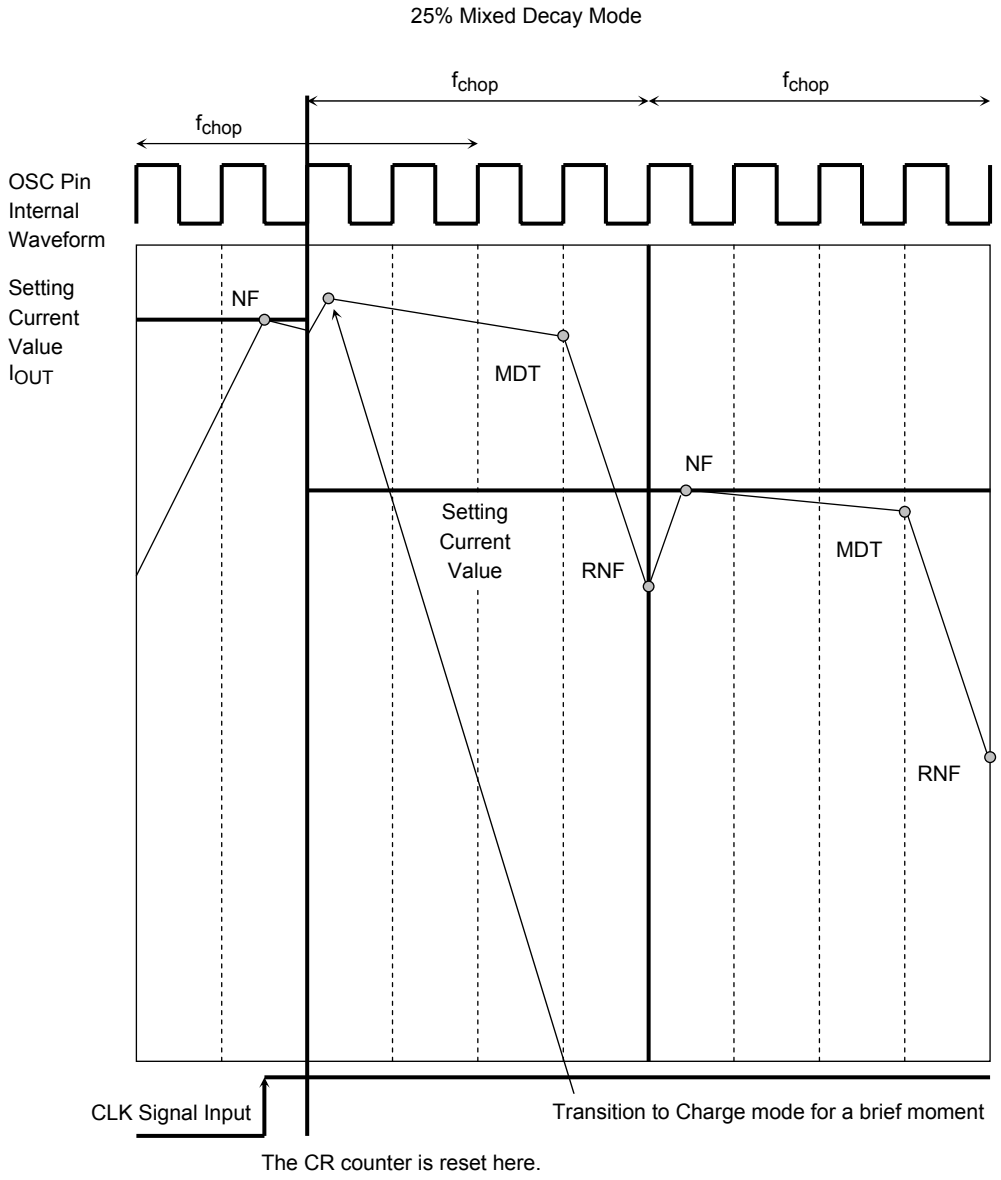
*: Even if the output current rises above the setting current at the RNF point, a charge is applied momentarily to confirm the current.

4. Fast Decay Mode Waveform

After the current value set by RNF, torque or other means is attained, the output current to load will make the transition to full regenerative mode.



5. CLK Signal and Internal CR CK Output Current Waveform (when the CLK signal is input in the middle of Slow mode)



When the CLK signal is input, the Chopping Counter (OSC Counter) is forcibly reset at the timing of the OSC.

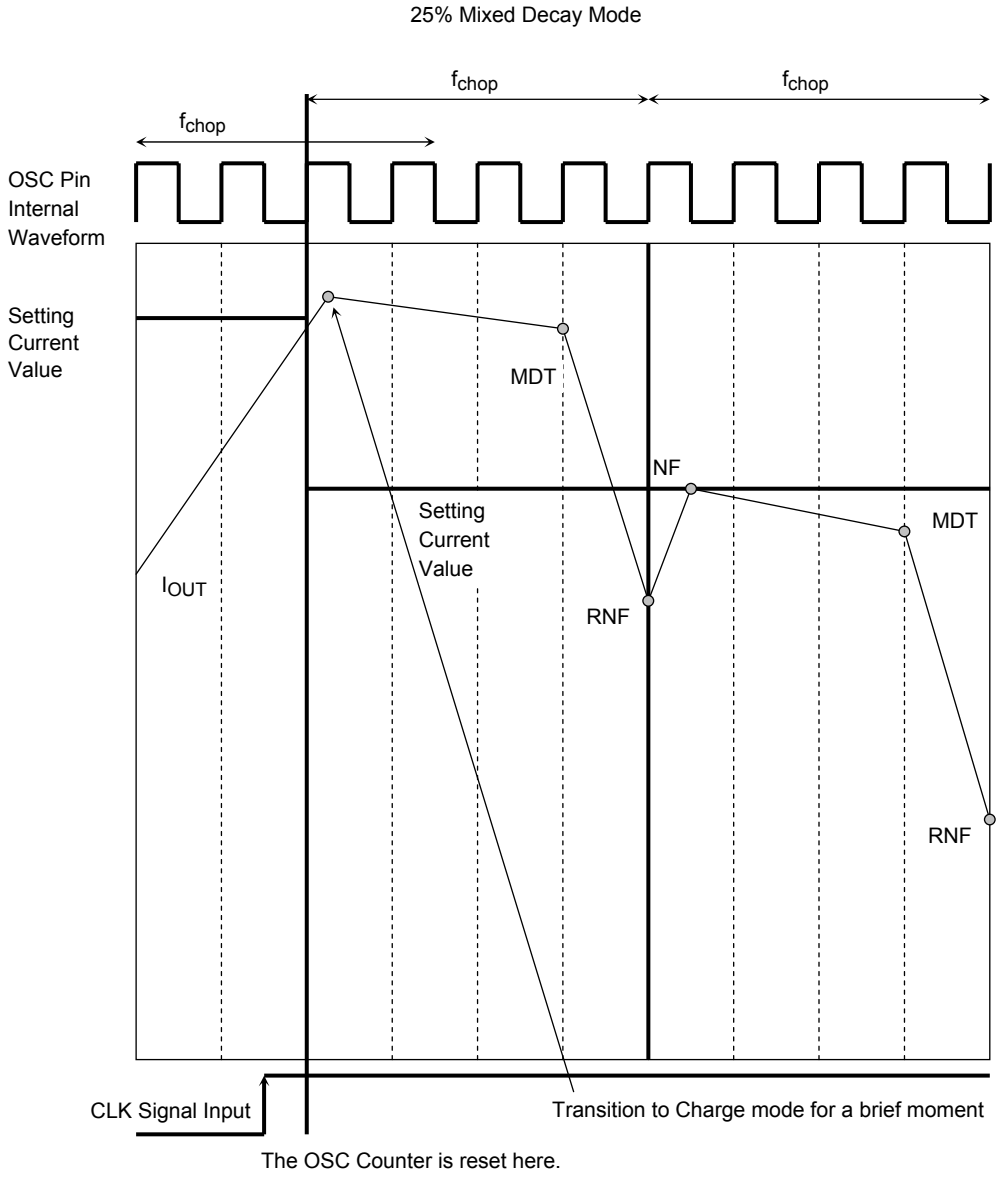
As a result, the response to input data is fast in comparison to methods that don't reset the counter.

The delay time is one OSC cycle: 10 μs @100 kHz Chopping using the Logic Block logic value.

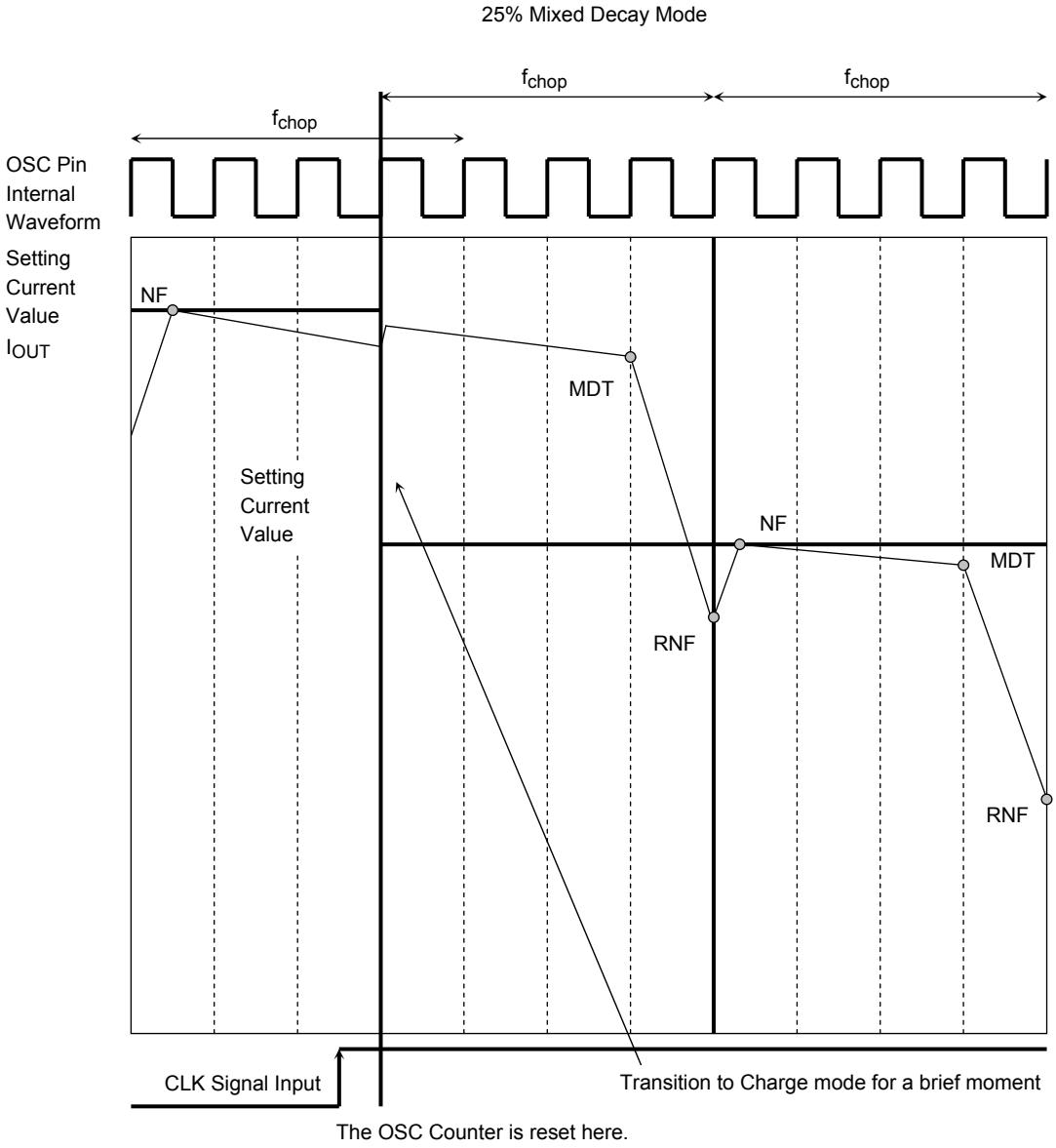
After the OSC Counter is reset by CLK signal input, the transition is invariably made to Charge mode for a brief moment to compare the current.

Note: Even in Fast Decay Mode, the transition is invariably made to Charge mode for a brief moment to compare the current.

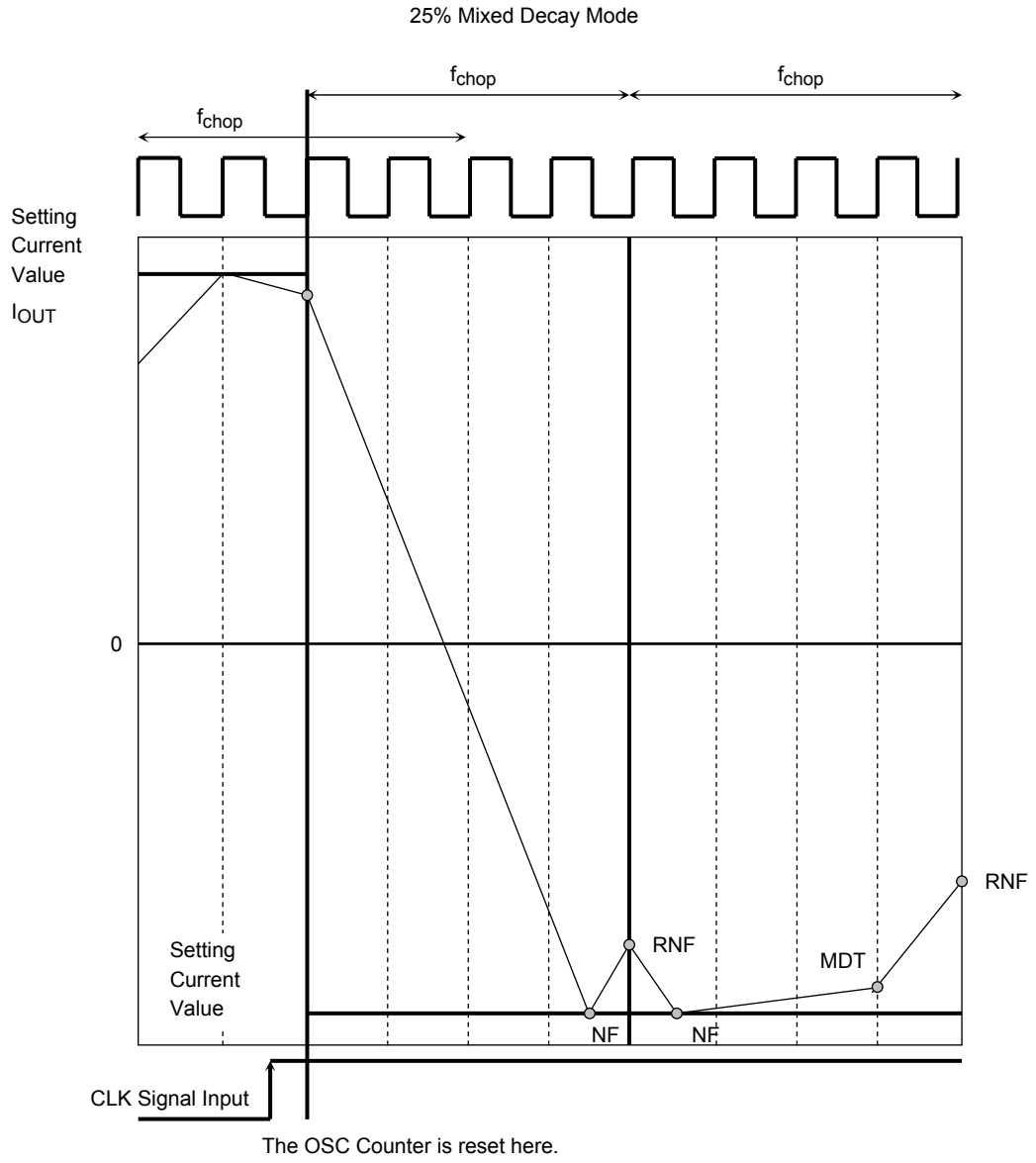
6. CLK Signal and Internal OSC Output Current Waveform (when the CLK signal is input in the middle of Charge mode)



7. CLK Signal AND Internal OSC Output Current Waveform (when the CLK signal is input in the middle of Fast mode)



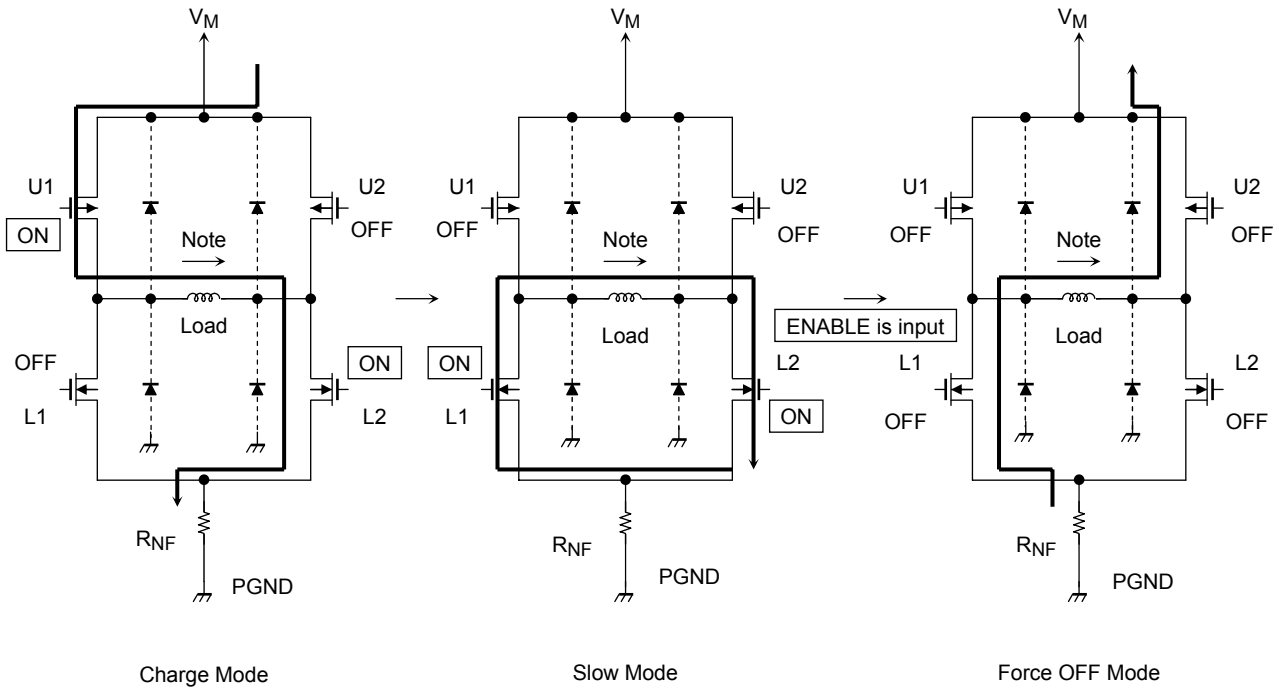
8. Internal OSC Output Current Waveform when Setting Current is Reverse (when the CLK signal is input using 2-phase excitation)



Current Draw-out Path when ENABLE is Input in Mid Operation

When all the output transistors are forced OFF during Slow mode, the coil energy is drawn out in the following modes:

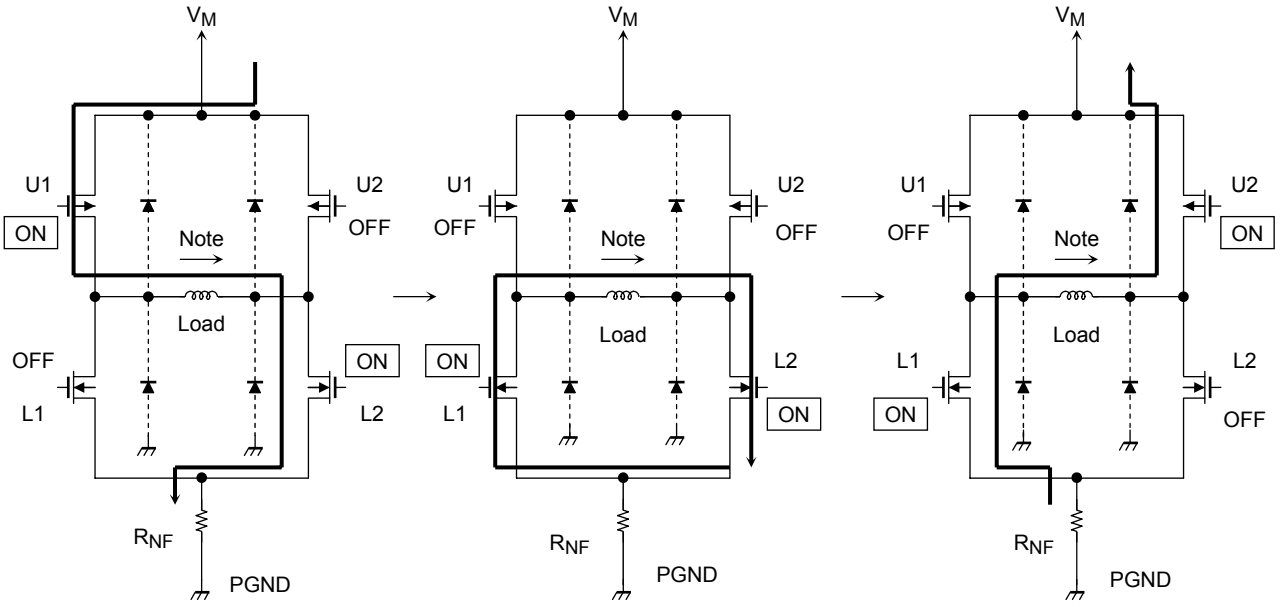
Note: Parasitic diodes are indicated on the designed lines. However, these are not normally used in Mixed Decay mode.



As shown in the figure above, an output transistor has parasitic diodes.

Normally, when the energy of the coil is drawn out, each transistor is turned ON and the power flows in the opposite-to-normal direction; as a result, the parasitic diode is not used. However, when all the output transistors are forced OFF, the coil energy is drawn out via the parasitic diode.

Output Stage Transistor Operation Mode



Charge Mode Slow Mode Fast Mode

Output Stage Transistor Operation Functions

CLK	U1	U2	L1	L2
CHARGE	ON	OFF	OFF	ON
SLOW	OFF	OFF	ON	ON
FAST	OFF	ON	ON	OFF

Note: The above chart shows an example of when the current flows as indicated by the arrows in the above figures. If the current flows in the opposite direction, refer to the following chart:

CLK	U1	U2	L1	L2
CHARGE	OFF	ON	ON	OFF
SLOW	OFF	OFF	ON	ON
FAST	ON	OFF	OFF	ON

Upon transitions of above-mentioned functions, a dead time of about 300 ns is inserted respectively.

Measurement Waveform

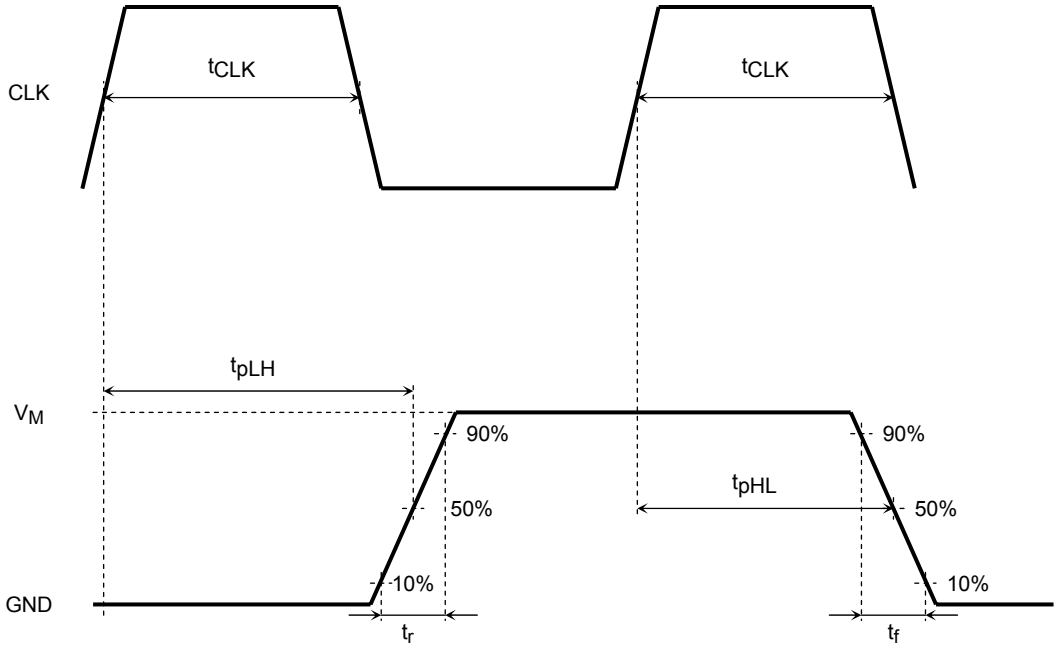


Figure 1 Timing Waveforms and Names

OSC-Charge DELAY:

The conversion from the OSC waveform to the internal OSC waveform is done by recognizing the level of chopping wave. The voltages of 2 V or above are considered as a High level, and voltages of 0.5 V or below are considered as a Low level as designed values. However, there is a response delay and that there occurs the peak-to-peak voltage variation.

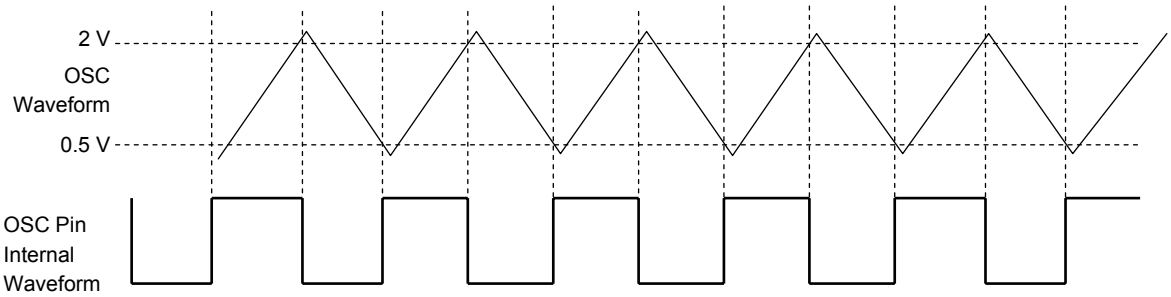
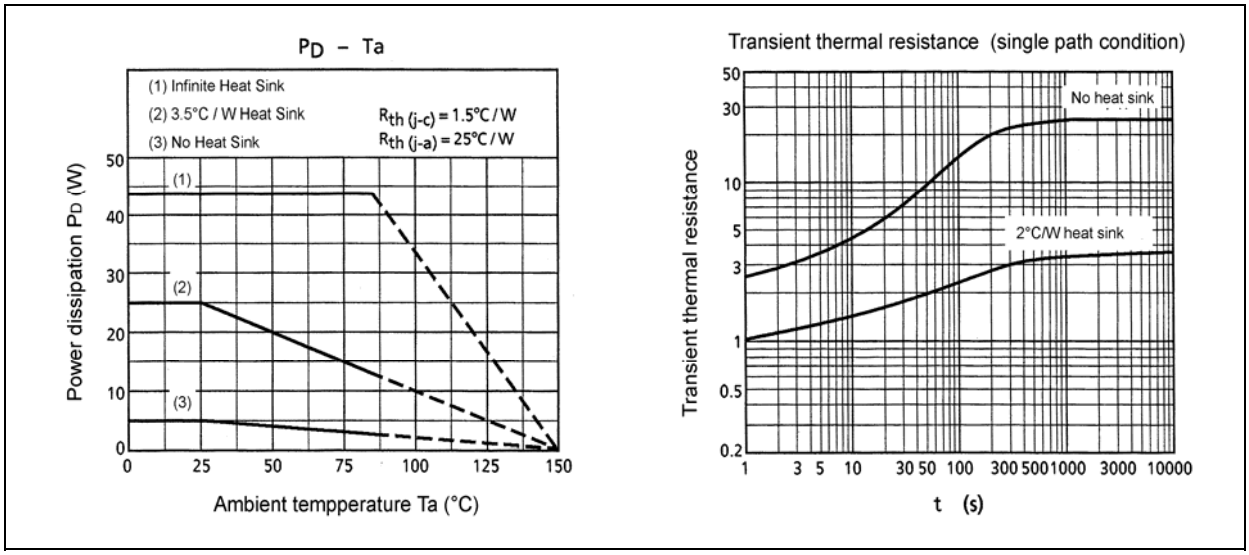


Figure 2 Timing Waveforms and Names (CR and Output)

Power Dissipation

TB6560AHQ



1. How to Turn on the Power and Input the Signal

Turn on V_{DD}. When the voltage has stabilized, turn on $V_{MA/B}$.
In addition, set the Control Input pins to Low when inputting the power.
(All the Control Input pins are pulled down internally.)

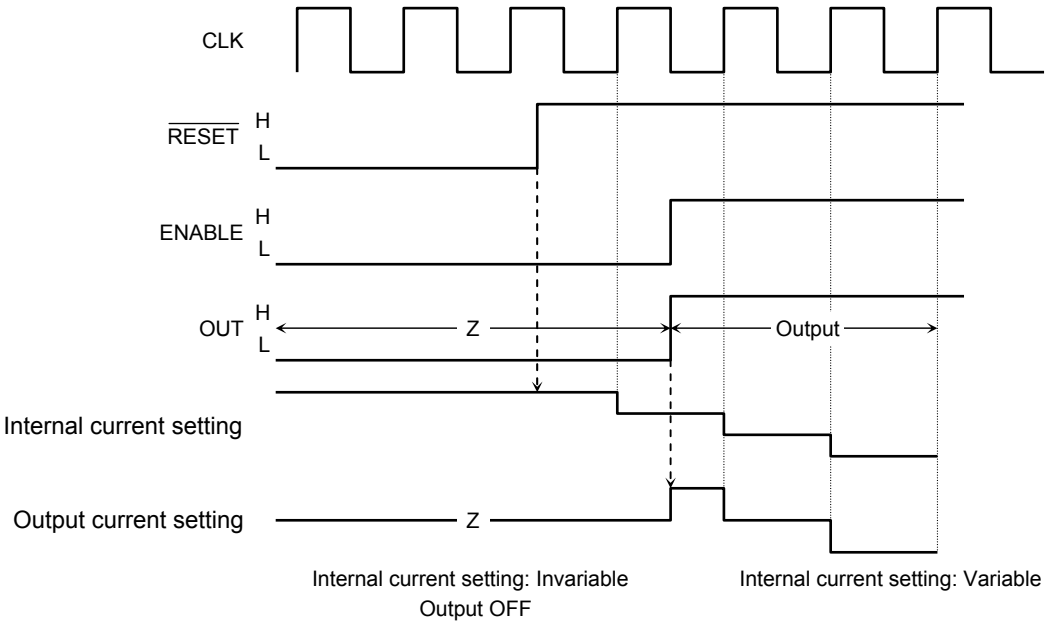
After V_{DD} and $V_{MA/B}$ reach the specified voltage completely, $\overline{RESET}$ and ENABLE can be set high. If you skip any of this process, the IC may not drive correctly and the IC and the peripheral parts may be destroyed.

Once the power is on, the CLK signal is received and excitation advances when $\overline{RESET}$ goes high and excitation is output when ENABLE goes high. If only $\overline{RESET}$ goes high, excitation won't be output and only the internal counter will advance. Likewise, if only ENABLE goes high, excitation won't advance even if the CLK signal is input and it will remain in the initial state.

The following is an example:

In shutdown the power, follow the inverse process.

<Recommended Control Input Sequence>



2. Power Dissipation

The IC power dissipation is determined by the following equation:

$P = V_{DD} \times I_{DD} + I_{OUT} \times Ron \times 2$ drivers

The higher the ambient temperature, the smaller the power dissipation.
Check the PD-Ta curve, and be sure to design the heat dissipation with a sufficient margin.

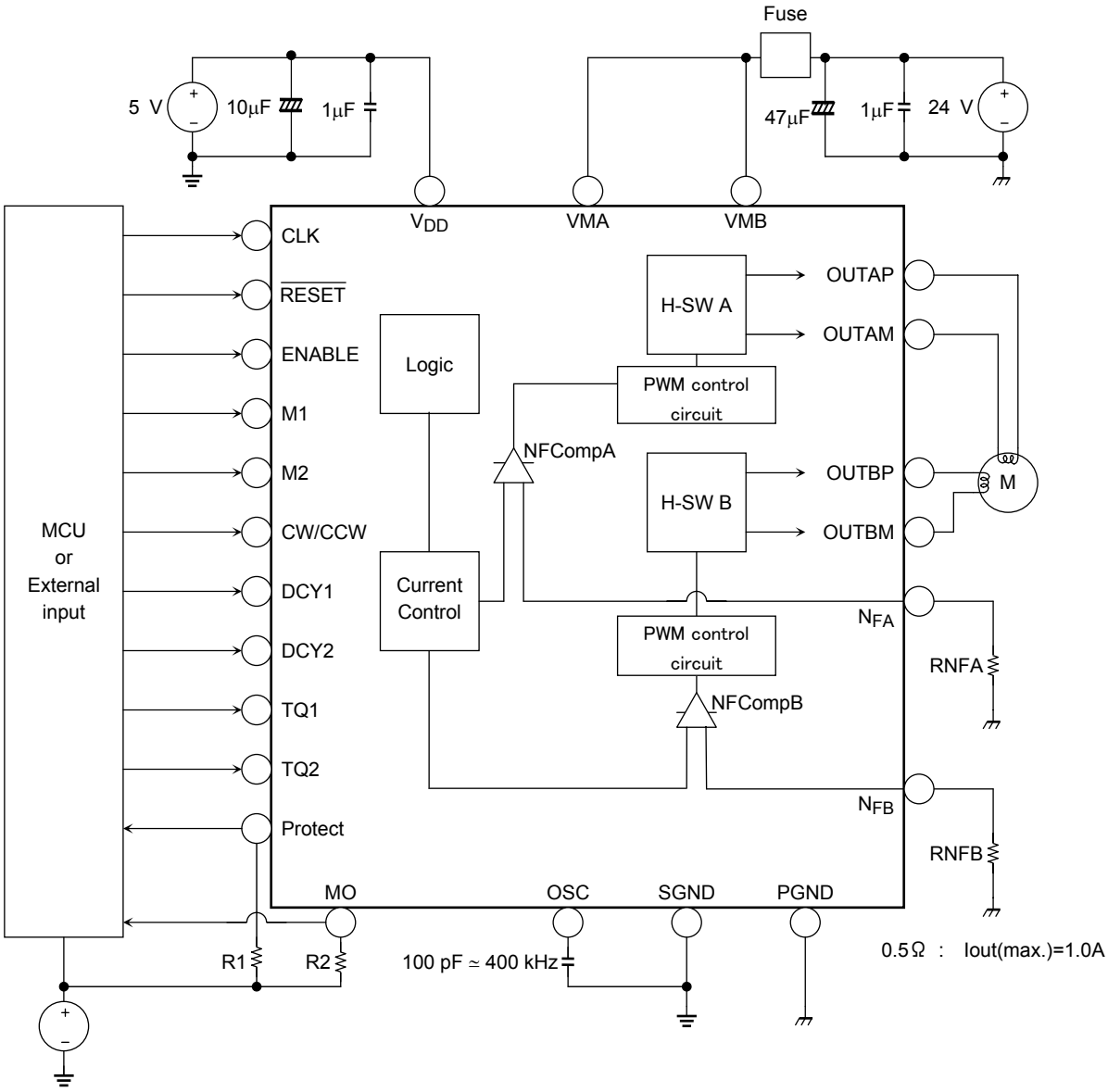
3. Heat Sink Fin Processing

The IC fin (rear) is electrically connected to the rear of the chip. If current flows to the fin, the IC will malfunction. If there is any possibility of a voltage being generated between the IC GND and the fin, either ground the fin or insulate it.

4. Thermal Protection

When the temperature reaches 170°C (as standard value), the thermal protection circuit is activated switching the output to off. There is a variation of plus or minus about 20°C in the temperature that triggers the circuit operation.

Application Circuit

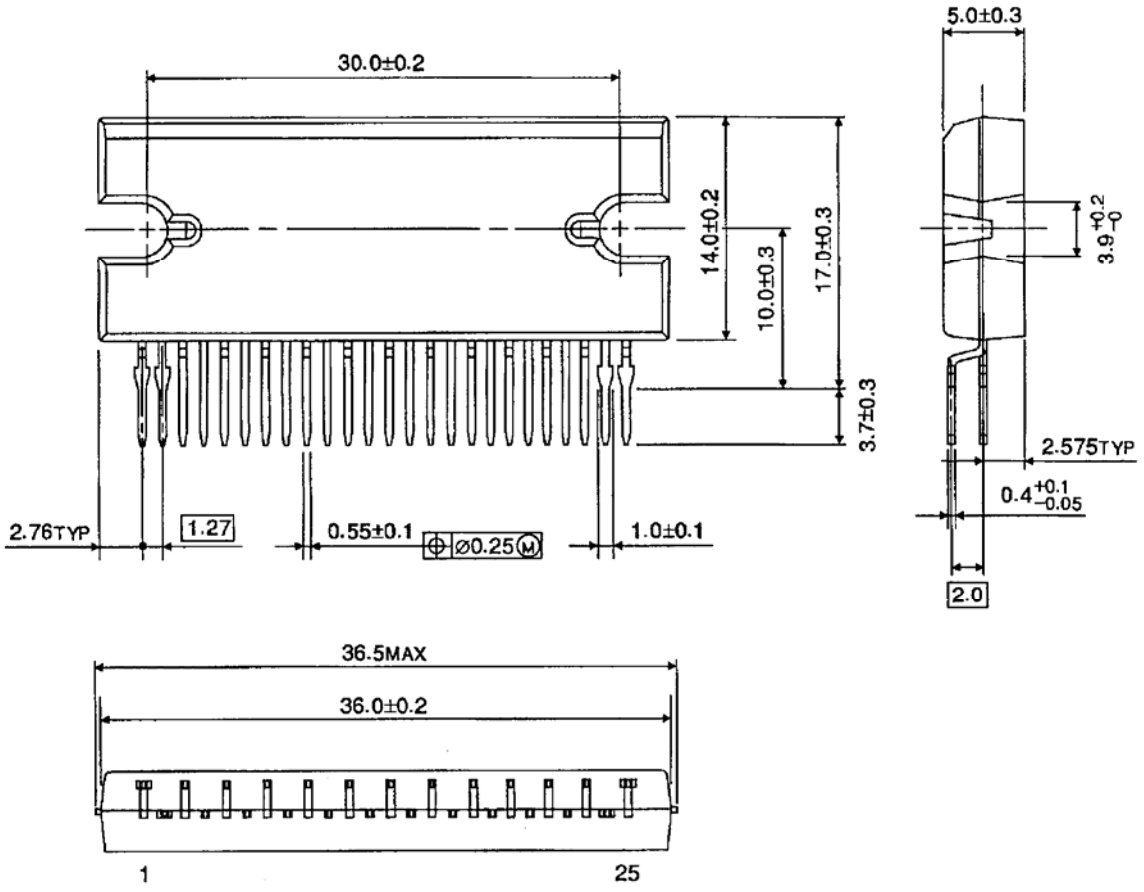


Note: Connect the power condenser to the IC as near as possible.

- Utmost care is necessary in the design of the output, V_{DD}, V_M, and GND lines since the IC may be destroyed by short-circuiting between outputs, air contamination faults, or faults due to improper grounding, or by short-circuiting between contiguous pins.
- Follow the process of inputting power described in page 28.

Package Dimensions

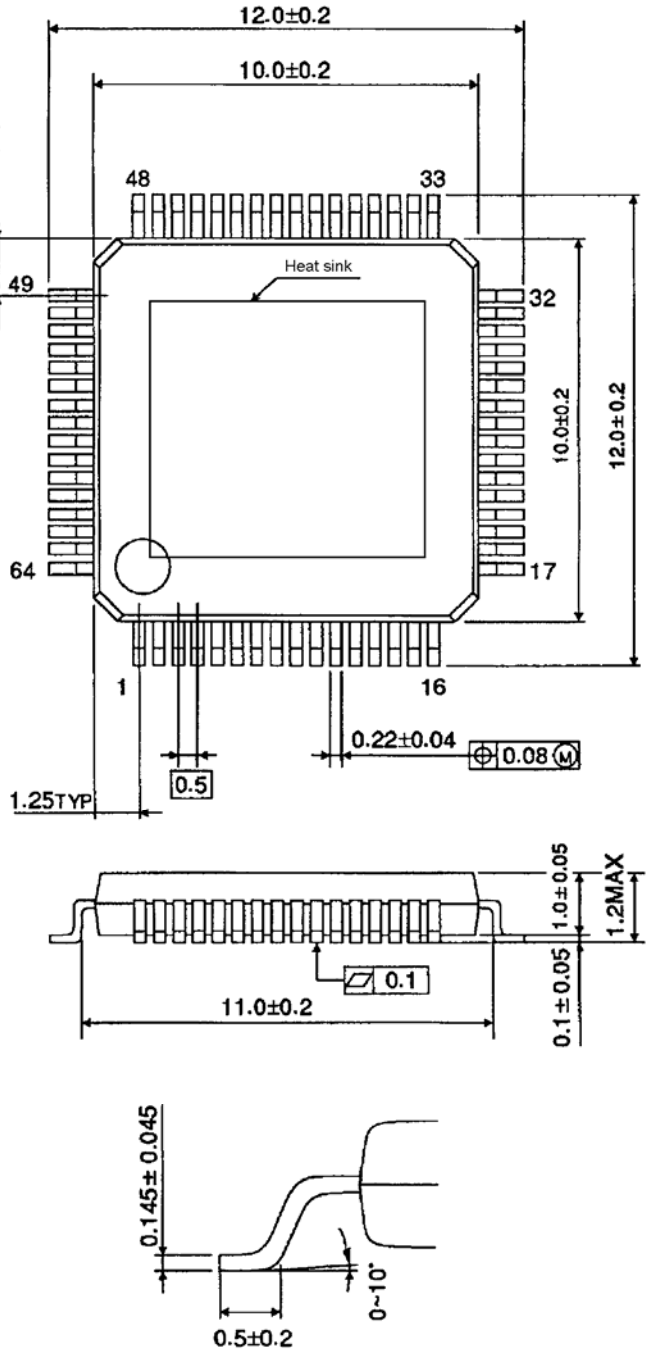
HZIP25-P-1.27 Unit : mm



Weight: 9.86 g (typ.)

Package Dimensions

HQFP64-P-1010-0.50 Unit : mm



Weight: 0.26 g (typ.)

Note: The rear heat sink block will be 5.5 mm × 5.5 mm. (PROVISIONAL)

Notes on Contents

1. Block Diagrams
Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

2. Equivalent Circuits
The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

3. Timing Charts
Timing charts may be simplified for explanatory purposes.

4. Application Circuits
The application circuits shown in this document are provided for reference purposes only. Thorough evaluation is required, especially at the mass production design stage.
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5. Test Circuits
Components in the test circuits are used only to obtain and confirm the device characteristics. These components and circuits are not guaranteed to prevent malfunction or failure from occurring in the application equipment.

IC Usage Considerations
Notes on handling of ICs

[1] The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.
Exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.

[2] Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead smoke or ignition. To minimize the effects of the flow of a large current in case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.

[3] If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition.
Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.

[4] Do not insert devices in the wrong orientation or incorrectly.
Make sure that the positive and negative terminals of power supplies are connected properly. Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.
In addition, do not use any device that is applied the current with inserting in the wrong orientation or incorrectly even just one time.

Points to remember on handling of ICs

(1) Thermal Shutdown Circuit

Thermal shutdown circuits do not necessarily protect ICs under all circumstances. If the thermal shutdown circuits operate against the over temperature, clear the heat generation status immediately.

Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the thermal shutdown circuit to not operate properly or IC breakdown before operation.

(2) Heat Radiation Design

In using an IC with large current flow such as power amp, regulator or driver, please design the device so that heat is appropriately radiated, not to exceed the specified junction temperature (T_J) at any time and condition. These ICs generate heat even during normal use. An inadequate IC heat radiation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, please design the device taking into considerate the effect of IC heat radiation with peripheral components.

(3) Back-EMF

When a motor rotates in the reverse direction, stops or slows down abruptly, a current flow back to the motor's power supply due to the effect of back-EMF. If the current sink capability of the power supply is small, the device's motor power supply and output pins might be exposed to conditions beyond maximum ratings. To avoid this problem, take the effect of back-EMF into consideration in system design.

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20070701-EN

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