Application Notes

EM198810 RF Transceiver Register Definitions

Add EM198810 recommend register setting (Appendix 1)

Programming RF Transceiver Registers

All registers of RF Transceiver can only be accessed using DBus serial interface protocol as described in EM198810 specification or EM198810 application note AN-198810-3 or SPI interface format.

Register descriptions

Receive RF Control (Write/Read) – Register 0 (Default =0xCD51)

Bit No.	Bit Name	Description
15 – 11	MIXER_GAIN[4:0]	Set 5-bit gain value for RX mixer.
10	MIXER_LP	“1”Enable RX mixer low-power mode.
9 - 5	RX_BPF_Q[4:0]	Set 5-bit Q value for band pass filter.
4-0	RX_BPF_GN1[4:0]	Set 5-bit gain value for the portion 1 receiver’s band pass filter.

RF Status (Read only) – Register 1

Bit No.	Bit Name	Description
15	VPON	One of the two indicators tells if the right VCO curve is selected.
14	VTFREQ	The other indicator tells if the right VCO curve is selected; both “VPON” and “VTFREQ” will be “1” when the right VCO is selected.
13-8	RC[5:0]	6-bit BPF RC calibrated value generated by RC CALC circuit.
7-0	ADC_DOUT[7:0]	8-bit values generated by A/D converter.

RF Synthesizer/VCO Configure (Write/Read) – Register 2 (Default = 0x137B)

Bit No.	Bit Name	Description
15	FORCE_IDLE	When “1’ to reset the digital modem into the idle mode
14	BYPASS_VCO_CAL	Disable automatic VCO curve calibration feature during Power-on state or Idle state. This bit takes precedence over VCO_CAL_EN (bit 1 of Register 26).
13	Reserved	
12	DEVIATION_SEL	“1” : select 320KHz deviation; “0” : select 160KHz deviation.
11-8	VCO_FC[3:0]	Set 4-bit value for TX modulator bandwidth; i.e. those 4 bits are for VCO Fc control.
7-4	VPON_TUNE[3:0]	Set VPON voltage step.
3-0	VTFREQ_TUNE	Set VTFREQ voltage step.

TX/RX Status (Read only) – Register 3

Bit No.	Bit Name	Description
15 – 11	BLUE_RF_STATE[4:0]	Show up the status of BlueRF finite state machine.
10	RC_FIN	RC finish status from RC CALC circuit.
9 - 6	VCO_CAL[3:0]	Indicate the current VCO frequency band setting after automatic calibration.
5	VCO_CAL_ERROR	An error flag indicates that no proper VCO curve can be found.

4	RF_SYNTH_LOCK	Indicate the lock status of RF synthesizer.
3 - 0	TEMP_SENSOR[3:0]	Indicate the current temperature range.

BLUE_RF_STATE

BLUE_RF_STATE [4:0]	STATE
00000	Off
00001	PwrOnWaitXTL
00010	HoldXTL
00011	Idle
00100	Sleep
00101	SleepWaitXTL
00110	VCO_Sel
00111	VCO_Wait
01000	RXPLLWait1
01001	RXPLLWait2
01010	RXWideFilt
01011	RXNarrowFilt
01111	VCO_PwrOnWait
10000	WaitDataSync1
10001	WaitDataSync2
10010	DataSync
10011	EnblePA1
10100	EnblePA2
10101	TXData
10110	DisablePA1
10111	DisablePA2
11000	DisablePA3

RF TX Control (Write/Read) – Register 4 (Default = 0x3CD0)

Bit No.	Bit Name	Description
15-14	RSSI_GN_ADJ[1:0]	RSSI control signal.
13-10	TXDAC_DC[3:0]	Set 4-bit value for TXDAC DC voltage level.
	RSSI_DIS	“1”:disable RSSI feature.
8	Reserved	
7-3	TXDAC_GAIN[4:0]	Set 5-bit gain value for TXDAC.
2-0	BG_TBIT[2:0]	Set 3-bit test-mode control for BandGap reference.

RX Timing/Power Control (Write/Read) – Register 5 (Default = 0x0081)

Bit No.	Bit Name	Description
15 – 11	SYNTH_ON_DELAY_CNT[4:0]	In the state “WAIT DATA SYNC” of BLUE RF, RF oscillator will be enabled at first. There is a time offset controlled by the counter SYNTH_ON_DELAY_CNT. When the counter counts to zero and SYNTH_IDLE_OFF = “0”, the synthesizer will be enabled. Each time increment is 1uS.
10 - 9	Reserved	
8	REG_PROTECT	The bit is used to protect the test registers from the access of Thunder users. Except Register 7, 8, 9, 30, 31 and REG_PROTECT, other Registers are protected by setting REG_PROTECT as “1”. When the value of REG_PROTECT is “0”, all the registers can be normally access.
7 – 0	RX_DELAY [7:0]	8-bit Receive delays from receiving synthesizer program register to start transmit BDATA1 to BBIC. Each time increment is 1uS.

TX Coefficient/RSSI Value (Read only) – Register 6

Bit No.	Bit Name	Description
15 – 10	RAW_RSSI[5:0]	Indicate 4-bit raw RSSI values from analog circuit for internal debugging purpose.
9	AGC	Indicate the current 1-bit AGC value. (See also Registers 14 and 17.)
8	RSSI_VALID	Indicate if the current RSSI value (bit 3-0 of this register) is valid.
7 - 0	RSSI[7:0]	Indicate the current 8-bit RSSI values.

RF Synthesizer / TX-RX Control (Write/Read) – Register 7 (Default = 0x0030)

Bit No.	Bit Name	Description
15 - 14	Reserved	
13 - 9	SWALLOW [4:0]	5-Bits Synthesizer Swallow counter. When the RF_PLL_DIRECT is set to “1”, the synthesizer will be programmed directly with Register7[13:9] and Register7[6:0]. The frequency of synthesizer will not be programmed as f = 2402+ PLL_CH_NO again.
8	DBUS_TX_EN	Enable the Transmit Sequence for state machine control.
7	DBUS_RX_EN	Enable the Receive Sequence for state machine control. Note that DBUS_TX_EN and DBUS_RX_EN cannot be “HIGH” at the same time; otherwise, the configuration to Thunder cannot work.
6 - 0	RF_PLL_CH_NO [6:0] /RF_PLL[6:0]	7 bits stand for the Bluetooth RF channels. The channel frequency will be: f = 2402+ PLL_CH_NO. When the RF_PLL_DIRECT is set to “1”, the synthesizer will be programmed directly with Register7 [13-9] and Register7[6:0]. Register7[6:0] are used as 7-bits Synthesizer Program counter The frequency of synthesizer will not be programmed as f = 2402+ PLL_CH_NO again.

RF_TX_EDR Control (Write/Read) – Register 8 (Default = 0x0404)

Bit No.	Bit Name	Description
15-13	Reserved	
12-8	ldo_lp_sleep[3:0]	Set 5-bit LDO sleep current.
7-5	Reserved	
4-0	Ldo_sp-normal[4:0]	Set 5-bit LDO operating current.

RFIC Control (Write/Read) – Register 9 (Default = 0x0404)

Bit No.	Bit Name	Description
15--12	PA_PWCTR[3:0]	PA high power version.
11 – 7	PA_GN[4:0]	5-bit transmit power amplifier gain setting.
6	TR_SW_POLARITY	When “0”, the default polarity of TR_SW is selected (TR_SW: “0” is for transmitting; “1” is for receiving); “1” the polarity of TR_SW is inverse.
5	APLL_VT_SENSE	APLL VT sense bit.
4	APLL_VT_FORCE	APLL VT force bit.
3	APLL_BP	Analog PLL Bypass mode. When “1”, Fout = Fin.
2	APLL_PDN	Analog PLL power-down mode. When “1”, APLL is power-off .
1	BRCLK_SEL	The selection pin for the BRCLK. If BRCLK_SEL = “1”, BRCLK = crystal_out or If BRCLK_SEL = “0”, BRCLK = TXCLK(1MHz). (default = “1”)
0	BRCLKEN	The output of BlueRF interface BRCLK works when BRCLKEN is high.(default = “1”)

AMS TEST Control (Write/Read) – Register 10 (Default = 0x0404)

Bit No.	Bit Name	Description
15	ENTER_SLEEP	When “1” is given, chip will enter into sleep mode to save power.
14	AMS_TST_ENB	When “1” is given, enable the AMS test mode and bypass BlueRF finite state machine.
12-13	AMS_TST_MD_SEL	00 : Normal operation mode, 01 : Enable the test for the digital to analog converter of the transmit I channel. 10 : Enable the test for the digital to analog converter of the transmit Q channel. 11 : Enable the test for the analog to digital converter of the RSSI.
11	TXDAC_MOD_MON	Enable DAC output monitor enable.
10	BPF_TST_PD	When”1”, indicate to power down the band pass filter during AMS_TST_ENB=”1”.
9-8	Reserved	
7	Ext_pa_sel	0: RXDATA=EXT_PA_CTRLo, Test1=EXT_TR_SWb, teste=EXT_TR_SWb. 1: RXDATA, Test1, teste back to previous define.
6	Reserved	
5	LNA_TST_PD	When “1”, indicate to power down LNA during AMS_TST_ENB=”1”.
4	ADC_TST_PD	When “1”, indicate to power down ADC during AMS_TST_ENB=”1”.
3	RF_VCO_TST_PD	When “1” is given, indicate to power down the RF VCO circuits during AMS_TST_ENB=”1”.
2	RC_TST_START	Provide test value for RC START during AMS_TST_ENB=”1”.
1	RC_TST_PD	When “1”, indicate to power down RC circuits during AMS_TST_ENB=”1”.
0	MIXER_TST_PD	When “1”, indicate to power down mixer during AMS_TST_ENB=”1”.

AMS TEST Control (Write/Read) – Register 11 (Default = 0x4041)

Bit No.	Bit Name	Description
15	TX_DAC_TST_PD	When “1” is given, indicate to power down the TX DAC during AMS_TST_ENB = “1”.
14	AMS_BUF_PD	Power down control for testing buffer in mixed-mode region. “1” means to power down, and “0” means in Testing mode.
13	AMS_BUF_LS	Signal level shift control for testing buffer in mixed-mode region. When “1” is given, the signal level will be shifted to 0.6V; in the another case (“0”), there are no any shift.

12	AMS_BUF_GN	Gain control for testing buffer in mixed-mode region. “1” →2V/V; “0” →1V/V.
11	AMS_BUF_SIN	Single-end input control for testing buffer in mixed-mode region. “1”→single end; “0”→difference mode.
10	reserved	
9	RSSI_PDN	“1”: power down RSSI.
8	reserved	
7	TX_PA_TST_PD	When “1”, indicate to power down the Power Amplifier module circuits during AMS_TST_ENB= “1”.
6	TR_TST_SW	When “1”, indicate to put the RF switch for the receiver and “0” for TX transmission path during AMS_TST_ENB = “1”.
5	ADC_TST_CLKEN	When “1”, provide enable signal to ADC clock enable input during AMS_TST_ENB = “1”
4	SYNTH_TST_PD	When “1” is given, indicate to power down the synthesizer circuits during AMS_TST_ENB =“1”.
3	reserved	
2	VCO_PDN	“1” : power down VCO.
1	PDN	“1” : power down synthesizer.
0	XTAL_OSC_EN	When “1” is set, enable the internal oscillator circuit.

AMS TEST Control (Write/Read) – Register 12 (Default = 0x0000)

Bit No.	Bit Name	Description
15-6	resv[15:0]	Reserved register to digital interface.
5-0	XI_trim[5:0]	For trim crystal.

AMS TEST Control (Write/Read) – Register 13 (Default = 0x0000)

Bit No.	Bit Name	Description
15-0	AMS_SW_SEL[15:0]	Switch selection control for mixed-signal circuit region. Note that this selection control is independent of AMS_TST_ENB.

AMS TEST Control (Write/Read) – Register 14 (Default = 0x0000)

Bit No.	Bit Name	Description
15-12	AG_TH[3:0]	Set high-bound threshold value for AGC.
11-8	AG_TL[3:0]	Set low-bound threshold value for AGC.
7	RX_BPF_LP	“1” : enable BPF and bpf1’s low power mode.
6	AGC_FORCE	“1” : force AGC to operate regardless of signal strength.(see also Register 6 and 17).
5	AGC_DISABLE	“1” : disable AGC circuit.
4-0	BPF_BW[4:0]	Set bandwidth value for receiver’s band pass filter.

RC Control (Write/Read) – Register 15 (Default = 0x017B)

Bit No.	Bit Name	Description
15	RC_SEL	Manually select RC value from bit 5-0 of this register.
14	rst_cnt2_sel	“1” : select 32, “0” : select 64.
13	rst_cnt3-sel	“1” : select 7, “0” : select 3.
12	rst_2_en	“1” : extra demod reset2 enable, “0” : reset2 disable, back to previous version.
11-6	RC_OFFSET[5:0]	Set 6-bit offset value for RC CALC circuit.
5-0	RC_MANU[5:0]	Manually select 6-bit RC value when RC_SEL is set.

BPF Control (Write/Read) – Register 16 (Default = 0xF000)

Bit No.	Bit Name	Description
15-13	RX_BPF_VO_Q[2:0]	Set 3-bit value to adjust the Q-path amplitude of band pass filter’s output.
12-8	RX_BPF_VO_I1[4:0]	Set 5-bit value to adjust the I-path amplitude of band pass filter’s output.(stage 1st)
7-3	RX_BPF_VO_I2[4:0]	Set 5-bit value to adjust the I-path amplitude of band pass filter’s output. (stage 2nd)
2-0	RX_BPF1_VO[2:0]	Set 3-bit value to adjust the amplitude of bpf1’s output.

AGC Control (Write/Read) – Register 17 (Default = 0x0000)

Bit No.	Bit Name	Description
15-0	Reserved	

TX/RX Data Control (Write/Read) – Register 18 (Default = 0xE000)

Bit No.	Bit Name	Description
15	SOFTWARE_CNTL	Set this bit to enable software to control the assertion time of PA_ON and SW_ON based on the values of TX_PA_ON_DELAY and TX_SW_ON_DELAY respectively; default setting ‘0’ is to select HW state machine to control those timing.
14	RX_DATA_INVERSE	The control signal provides the convenience for using the upper band or lower band of IF signal. When “1” is given, the polarity of the received signals BDATA1 or RXDATA will be inverse.
13	BYPASS_PLL_LOCK	When “1” is given, the transmitter will start to put the data on the air just after the time out of TX delay, and will not wait for the stable state of RF PLL.
12-10	TX_CW[2:0]	Set the time period to transmit CW bits in TX mode after TR_SW is on; when this time period expires, TX data from BB will be transmitted.
9	BRCLK_SW	“1” : route the 12M from APLL to BRCLK pin.
8	TX_DATA_INVERSE	When “1” is given, the polarity of the transmitting data BDATA1 will be inverse internally.
7-0	reserved	

DC Offset Control (Write/Read) – Register 19 (Default = 0x2114)

Bit No.	Bit Name	Description
15	reserved	LNA high power.
14	LOBUF_HP	PA high power.
13	ADC_LP	ADC low power.
12	Reserved	
11-9	Reserved	
8	Bpktctl_sel	1: BPKTCTL control wide mode to Narrow mode in receiving.
7-4	WIDE_TC[3:0]	Select the time period for DC offset wide mode; during this period, DC offset circuit will use the speed set by bit 3-2 to track DC offset values; after selected time period expires DC offset circuit will automatically switch to the speed of narrow mode (bit 1-0 of this register). Please note the tracking speed in wide mode will be always faster than in narrow mode.
3-2	WIDE_TRACK_SPED [1:0]	Set alpha value for DC offset tracking speed in RX wide mode.
1-0	NARROW_TRACK_ SPEED[1:0]	Set alpha value for DC offset tracking speed in RX narrow mode.

WIDE_TC

WIDE_TC [3:0]	Time Period(us)
0000	0
0001	8
0010	16
0011	24
0100	32
0101	40
0110	48
0111	56
1000	64
1001	72
1010	80
1011	88
1100	96
1101	104
1110	112
1111	120

WIDE_TRACK_SPEED

WIDE_TRACK [1:0]	Alpha Value
00	4 (slowest)
01	6
10	8
11	10 (fast)

NARROW_TRACK_SPEED

WIDE_TRACK [1:0]	Alpha Value
00	1 (slowest)
01	2
10	3
11	4 (fast)

PLL Synthesizer Control (Write/Read) – Register 20 (Default = 0x0003)

Bit No.	Bit Name	Description
15	PLL_FREQ_PLUS	Set to choose the upper sideband Low IF signal or lower sideband Low IF signal to be demodulated.
14-8	PLL_RX_FREQ_OFFSET	Set the RF PLL offset frequency above local oscillator.
7-5	A_INIT[2:0]	PLL A count initial value in power down mode.
4	SYNTH_LP	Set PLL low power.
3	LNA_LP	Set LNA low power.
2	LOBUF_LP	Set local oscillator buffer low power.

PLL Synthesizer Control (Write/Read) – Register 21 (Default 0x6962)

Bit No.	Description	Description
15	APLL_IDLE_OFF	1: APLL will be put into the power-off state in IDLE.
14	RF_VCO_IDLE_OFF	The RF VCO will be put into the power-off state if SYNTH_IDLE_OFF is “HIGH”; otherwise, they will be still active when SYNTH_IDLE_OFF is “LOW”.
13	SYNTH_IDLE_OFF	The Synthesizer will be put into the power-off state if SYNTH_IDLE_OFF is “HIGH”; otherwise, they will be still active when SYNTH_IDLE_OFF is “LOW”.
12	RF_PLL_DIRECT	When the RF_PLL_DIRECT is set to “1”, the synthesizer will be programmed directly with Register7[11:0]. The frequency of synthesizer will not be programmed as f = 2402+ PLL_CH_NO again.
11 – 0	PLL_RF_FREQ_BASE	Set the RF PLL base frequency.(Default = 2402 MHz)

TX RF Timing Control (Write/Read) – Register 22 (Default 0x2602)

Bit No.	Bit Name	Description
15 – 8	TX_PA_ON_DELAY	These registers are the initial value for the counter of the TX RF PA (Power Amplifier) power-on control. The counter begins to count to zero just after that TX RF modulator power-on was turn on in PA-ON state. When the counter is zero, PA will be active. Each time increment is1 uS; also these registers are to set the timing delay of the assertion of PA_ON after BPKTCTL is asserted, provided SOFTWARE_CNTL (bit 15 of Register 18) is set.
7 – 0	TX_PA_OFF_DELAY	These registers are the initial value for the counter of the TX PA power-off control. When the BLUE-RF state is in PA-OFF and the counter decreases to zero, TX PA will be turn OFF. Each time increment 1 uS.

TX RF/WAKE-UP Timing Control (Write/Read) – Register 23 (Default 0x0802)

Bit No.	Bit Name	Description
15 – 8	TX_SW_ON_DELAY	These registers are the initial value for the counter of the TR_SW selection control. After TX PA is ON, the counter begins to count to zero. When the counter is zero, the Transceiver Switch is moved to the TX path. Each time increment is1 uS, also these registers are to set the timing delay of the assertion of SW_ON after BPKTCTL is asserted, provided SOFTWARE_CNTL (bit 15 of Register 18) is set.
7 – 0	WAKE_UP_TIME	These registers are the initial value for the counter of the wake-up time control from the “SLEEP” mode to “IDLE” mode. After the signal BXTLEN is from low to high level, the counter begins to count to zero. Then, Thunder will enter “IDLE” state after counter is zero. Each time increment is 1 uS.

Fractional-N/VCO Control 1 (Write/Read) – Register 24 (Default 0xB040)

Bit No.	Bit Name	Description
15	APLL_LOCL	Read only
14	FORCE_DIT	“1” : unconditionally enable dithering feature.
13	DIT_P_EN	“1”: enable dithering feature only when phase interpolator counter’s value is between 0 to 7 or 56 to 63.
12	SEL_16_32	“0”: select add/subtract 16 in calculating sigma-delta outputs when dithering feature is enabled. “1”: select add/subtract 32 in calculating.
11-10	PRE_SCAL_DLY[1:0]	Time delay setting of MC signal to pre-scalar.
9-6	VCO_FB[3:0]	VCO frequency band setting.
5	VCO_VT_SENSE	VCO VTUNE sense bit; “1” enable sensing of VTUNE at VTUNE_IO pin.
4	Reserved	

Bit No.	Bit Name	Description
3	TEST_DIV	“1” : route DIV signal to PFD to SYNTH_SIGOUT pin.
2	TEST_FREF	“1” : route FREF signal to SYNTH_SIGOUT pin.
1	TEST_NA	“1” : route CLK of N/A counters to SYNTH_SIGOUT pin.
0	TEST1_OUT_EN	“1” : select TEST1 pin as the SYNTH_SIGOUT output for monitoring purpose.

Fractional-N/VCO Control 2 (Write/Read) – Register 25 (Default 0x7819)

Bit No.	Bit Name	Description
15-12	CLOSE_LP_DLY[3:0]	Select the delay of Gaussian filter outputs in order to compensate for the delay of Sigma-Delta modulator.
11	SEL_GAU_OUTPUT	“1”: select Gaussian filter output to feed into D/A during TX mode; “0”: select square wave output to feed into D/A during TX mode.
10	A_INIT_EN	PLL A count initial value enable.
9	SYN_FST_MODE_BP	“1” : Bypass Fast Mode of synthesizer.
8	SYN_FIN_SEL	Set internal 6MHz or 12MHz reference clock for synthesizer to save power.
7-6	T_RES1[1:0]	Reserved register 1 for RF control signals.
5-0	RCP0[5:0]	Charge pump current setting 0. This setting will be valid only when chip is in receiving mode.

CLOSE_LP_DLY

CLOSE_LP_DLY [2:0]	Delay (# of 12MHz clock)
000	4-clock delay
001	5-clock delay
010	6-clock delay
011	7-clock delay
100	8-clock delay
101	9-clock delay
110	10-clock delay
111	11-clock delay

Miscellaneous Control (Write/Read) - Register 26 (Default 0x6704)

Bit No.	Bit Name	Description
15-10	RCP1[5:0]	Charge pump current setting 1. This setting will be valid when chip is in transmitting mode.
9	VCO_ADJ_EN	“1” : enable automatic VCO adjustment logic.
8	VCO_VT_FORCE	Provide control signal to VCO VT.
7	TEST1_DIGI_SEL	“1”: route internal signal UPDATE to TEST1 pin for debug purpose; “0”: route internal signal ACCU_IN_MSB to TEST1 pin. Please note bit 0 of register 24 has the precedence over this bit.

Bit No.	Bit Name	Description
6	BYPASS_GAU	“1” : set to bypass digital Gaussian filter logic during TX mode.
5-3	VCO_BIAS[2:0]	VCO bias current setting.
2	VCO_FB_DIVSEL	“1”: enable 8 divisions of VCO frequency band setting for automatic VCO adjustment feature; “0”: enable 4 divisions of VCO frequency band setting for automatic VCO adjustment feature.
1	VCO_CAL_EN	Manually enable RFIC to start automatic VCO curve calibration procedure during Idle state.
0	AUTO_VCO_SEL	“1”: select CAL_VCO (bit 8-5 of Register 3) as effective VCO frequency band setting; “0”: select VCO_FB (bit 9-6 of Register 24) as effective VCO frequency band setting.

APLL Fractional Bus Value Control (Write/Read) - Register 27 (Default 0x0000)

Bit No.	Bit Name	Description
15-0	Reserved	

Reference Clock (Write/Read) - Register 28 (Default 0x1800)

Bit No.	Bit Name	Description
15-14	reserved	
13-0	REF_FQ[13:0]	Set crystal frequency; bit 13-9 represent the integer part of crystal frequency in binary expression and bit 8-0 represents the fractional part of crystal frequency in binary expression (bit 8 = 0.5; bit 7 = 0.25; bit 6 = 0.125,…., and so on).

Manufacture’s Revision Code (Read only) – Register 29 (Default 0x00?0)

Bit No.	Bit Name	Description
7-4	RF_VER_ID[15:0]	This field is used to identify the sub-revision of the design. 0000 means no rev letter; 0001 means rev A; 0010 means rev B; 0011 means rev C, etc.
3-0	Reserved	

Manufacture’s ID Code LSB (Read only) - Register 30 (Default 0x2413)

Bit No.	Bit Name	Description
15-0	ID_CODE_L[15:0]	Lower 16-bit of JEDEC JEP106-K Manufacture’s ID code, containing manufacturer, part number, and version. The LSB is always “1”.

Manufacture’s ID Code MSB (Read only) - Register 31 (Default 0x2184)

Bit No.	Bit Name	Description
15-12	RF_CODE_ID	
11-0	ID_CODE_M[31:16]	Upper 16-bit of Manufacture’s ID code.

EM198810 Framer Transceiver Register Definitions

CONFIGURE_REG Register 48 (default 0x5800):congig

Bit	Name	R/W	Description	default
15:13	Preamble_len	R/W	000: 1byte, 001: 2bytes, 010: 3 bytes, . . 111: 8 bytes Note: in transmit mode, always keep 8bit "1010…" before BPKTCTL as sync data.	010B
12:11	Syncword_len	R/W	11: 64 bits, {Reg55[15:0],Reg54[15:0],Reg53[15:0],Reg52[15:0]} 10: 48bits, {Reg55[15:0],Reg54[15:0],Reg52[15:0]} 01: 32bits, {Reg55[15:0],Reg52[15:0] 00: 16 bits,{Reg52[15:0]}	11B
10:8	Trailer_len	R/W	000: 4 bits, 001: 6bits, 010: 8 bits, 011: 10 bits . . 111: 18bits	000B
7:6	Data packet type	R/W	00: NRZ law data 01: Manchester data type 10: 8/10 line code 11: interleave date type	00B
5:4	FEC type	R/W	00: No FEC 01: FEC13 10: FEC23 11: reserved	
3	Power done	W	1: framer set BnPWR low to RFIC, than off the crystal buffer.	0B
2	Sleep mode	W	1: framer set BXTLEN low to RFIC, then off the crystal.	0B
1	Reset RFIC	W	1: MCU just to reset RFIC, once short.	0B
0	Fun_sel	W	1: framer off. 0: framer on.	0B

DELAY_REG0 Register 49 (default 0xC00F)

Bit	Name	R/W	Description	default
15:8	BXTLEN delay time	R/W	Max delay time? To define count step (Min~Max: 0.5~2ms) 1: 8us	C0H
7	Brclk_on_sleep	R/W	0: BRCLK is running at sleep mode.	0B
6	reserved			0B
5:0	BDATA1 delay time	R/W	After BXTLAN BDATA1 keep high time. 1:1us	0FH

DELAY_REG1 Register 50 (default 0x9628)

Bit	Name	R/W	Description	default
15:8	TX_dly_tim	R/W	FW write reg7 TX enable, after TX_dly_tim time, HW start transmit time. Unit: 1 means 1uS	96H
7:0	PA_dly_tim	R/W	PA on delay time after BPKTCTL driven high, Unit: 1 means 1uS	28H

DELAY_REG2 Register 51 (default 0x4000)

Bit	Name	R/W	Description	default
15:8	RX_dly_tim	R/W	FW write reg7 RX enable, After RX_dly_tim, HW start process received data via RXCLK Unit: 1 means 1uS	83H
7	Miso_tri-opt	R/W	0: SPI_MISO is tri-state when SPI_SS=1, 1: SPI_MISO keep output.	0B
6:0	Scramble_data	R/W		00H

SYNC_WORD_1 Register 52 (defult 0x0000)

Bit	Name	R/W	Description	default
15:0	SYNC_WORD[15:0]		LSB bits of sync word is first, it match the BT SPEC.? In different syncword length, this register is first send out.	0000H

SYNC_WORD_4 Register 53 (default 0x0000)

Bit	Name	R/W	Description	default
15:0	SYNC_WORD[31:16]		LSB bits of sync word is first	0000H

SYNC_WORD_3 Register 54 (default 0x0000)

Bit	Name	R/W	Description	default
15:0	SYNC_WORD[47:32]		LSB bits of sync word is first	0000H

SYNC_WORD_2 Register 55 (default 0x0000)

Bit	Name	R/W	Description	default
15:0	SYNC_WORD[63:48]		LSB bits of sync word is first	0000H

Threshold_reg Register 56 (default 0x4407)

Bit	Name	R/W	Description	default
15:12	TX_FIFO_threshold	R/W		0100B
11:8	RX_FIFO_threshold	R/W		0100B
7	Pkt_hint_pority	R/W	1: PKF-flag/FIFO_flag low active. 0: high active.	0B
6	addr_match_opt	R/W	Addr_match time option to fix RXCLK gitter.	0B
5:0	Syncword_threshold	R/W		07H

RF_CTRL Register 57 (default 0xB000)

Bit	Name	R/W	***Description***	default
15	CRC_on	R/W	0: CRC off. 1: CRC on	1
14	Scramble_on	R/W	0: scramble off. 1: scramble on	0
13	Pack_lenth_en	R/W	1: HW regards first byte payload is length	1
12	DIRECT_COTROL_MASK	R/W	1: RF status from off status to idle status is controlled by BNPWR_PIN, BXTLEN_PIN, BDATA1_PIN. 0: When REST_n = 1, waiting certain timing, RF status will be automatically enter idle status.	1
11	BNPWR_PIN	R/W		0
10	BXTLEN_PIN	R/W		0
9	BDATA1_PIN	R/W		0
8	Fw_term_tx	R/W	0:FW handle packet length and terminate TX by FW 1:when fifo write point equals read point, HW terminate TX when FW handle packet length	0
7:0	Crc initial data	R/W		00H

Reserve_reg Register 58 (default 0x0000)

Bit	Name	R/W	Description	default
15:0	reserved	R/W		00H

Main_status Register 64 (Read only)

Bit	Name	R/W	Description	default
15:12	Framer/RFIC_st	R	BnPWR, BXTLEN, TX_EN, RX_EN 0xxx: OFF status 1000: sleep staus 1100: Idle 1110: transmit 1101: receive others: illegal status	
11	Error_ok	R	1: have error in receiving Include FEC | CRC check, it will be cleared in next start RX/TX	
10	Syncword_rev	R	1: syncword received, it is just available in receive status, after out receive status, always keep '0'	
9:8	reserved			
7:4	Framer TX status	R	Come from HW TX state machine, also can help HW to debug.	
3:0	Framer RX status	R	Come from HW RX state machine.	

TX_FIFO_REG Register 80

Bit	Name	R/W	Description	default
15:0	TXRX_FIFO_REG	R/W	For MCU read/write data between the FIFO	00

Note: FW access FIFO is byte by byte.

FIFO_RD_PTR Register 82

Bit	Name	R/W	Description	default
15	Clr_w_ptr	W	1: clear TX FIFO point to 0 when write this bit to “1”. It is not available in RX status	0
14:8	FIFO_WR_PTR	R	FIFO write point.	
7	Clr_r_ptr	W	1: clear RX FIFO point to 0 when write this bit to “1”. It is not available in TX status	0
6:0	FIFO_RD_PTR	R	FIFO read point.	

Appendix 1: Recommend register setting for EM198810.

EM198810 recommended register setting table

RF initiation

Reg. address	Read/Write	Default value (Hexadecimal)	Recommend value (12MHz crystal frequency) (Hexadecimal)
0x09	R/W	3003	2001
0x00	R/W	CD51	354D
0x02	R/W	137B	1F01
0x04	R/W	3CD0	BCF0
0x05	R/W	0081	00A1
0x07	R/W	0030	124C
0x08	R/W	0404	8000
0x0C	R/W	0000	8000
0x0E	R/W	6697	169B
0x0F	R/W	017B	90AD
0x10	R/W	F000	B000
0x13	R/W	2114	A114
0x14	R/W	819C	8191
0x16	R/W	0402	0002
0x18	R/W	B040	B140
0x19	R/W	7819	A80F
0x1A	R/W	6704	3F04
0x1C	R/W	1800	5800

Framer initiation

Reg. address	Read/Write	Default value (Hexadecimal)	Recommend value (12MHz crystal frequency) (Hexadecimal)
0x30	R/W	5800	9800
0x31	R/W	C00F	FF8F
0x32	R/W	9628	8028
0x33	R/W	8300	8056
0x34	R/W	0000	4EF6
0x35	R/W	0000	F6F5
0x36	R/W	0000	185C
0x37	R/W	0000	D651
0x38	R/W	4407	4444
0x39	R/W	B000	E000

* Reg57, if MCU handle packet length and framer detect FIFO fully empty, Reg57=0xC080

* Reg57, if MCU handle packet length and terminates TX done, Reg57=0xC000